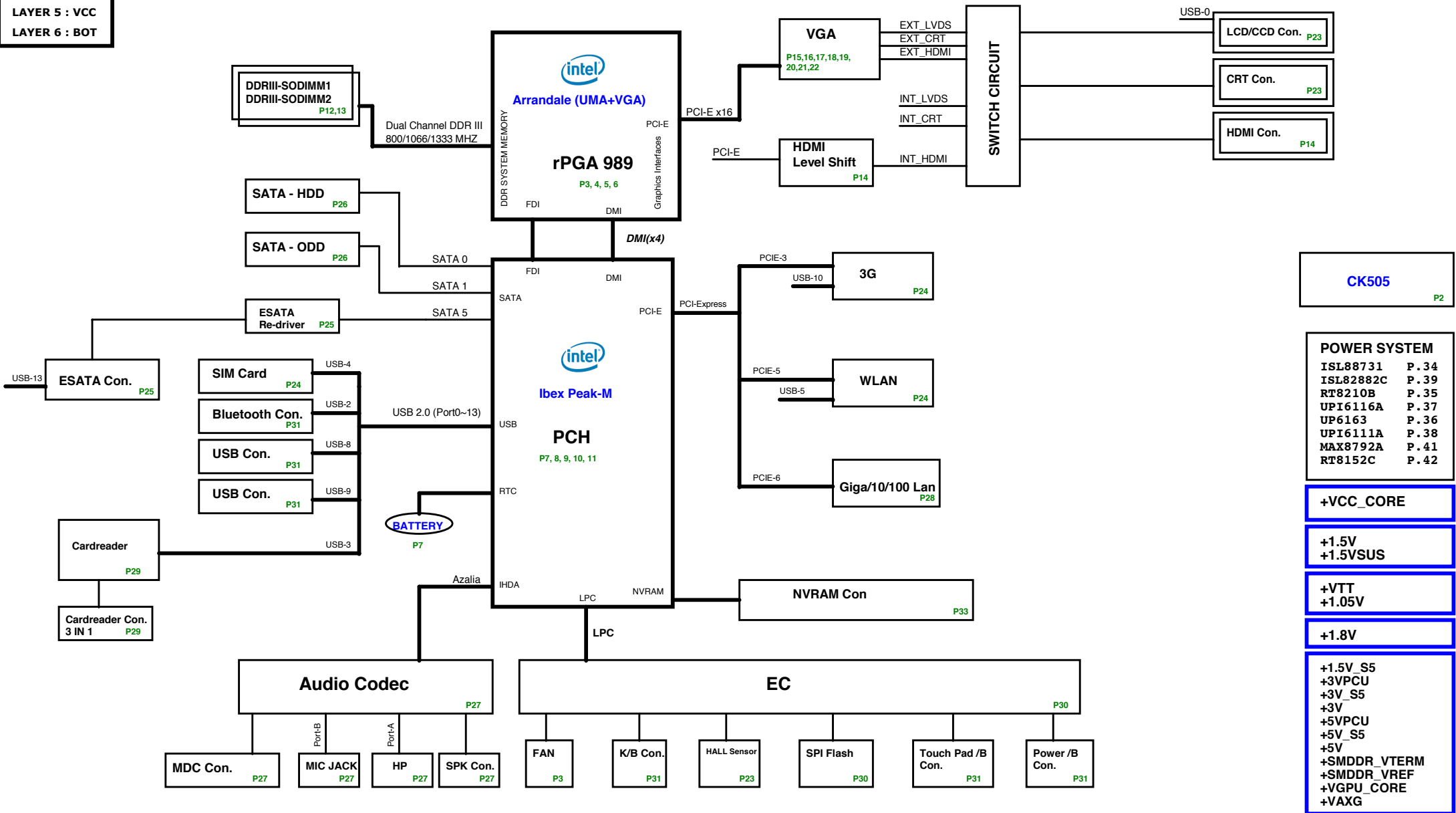
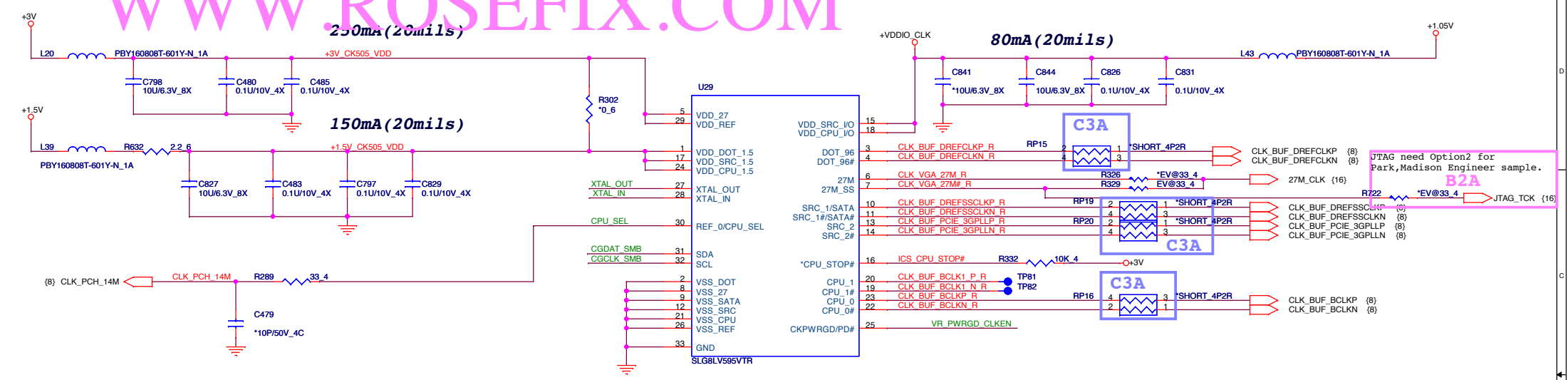


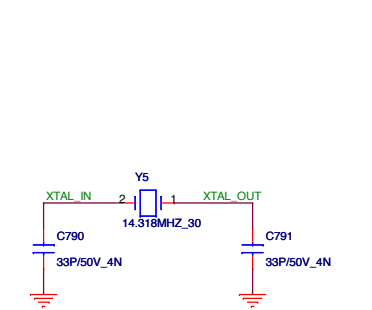
PCB STACK UP  
LAYER 1 : TOP  
LAYER 2 : GND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : VCC  
LAYER 6 : BOT

BL6 Block Diagram

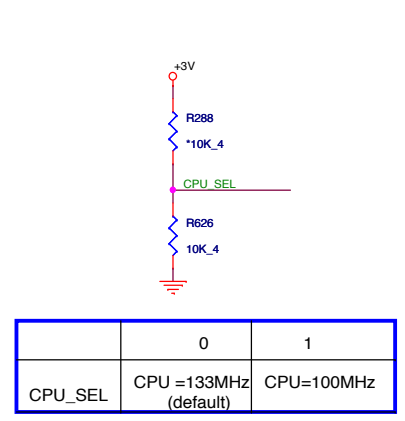




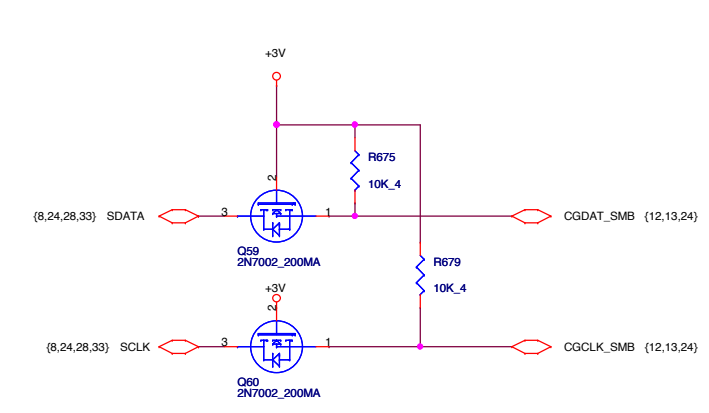
CLK CRYSTAL



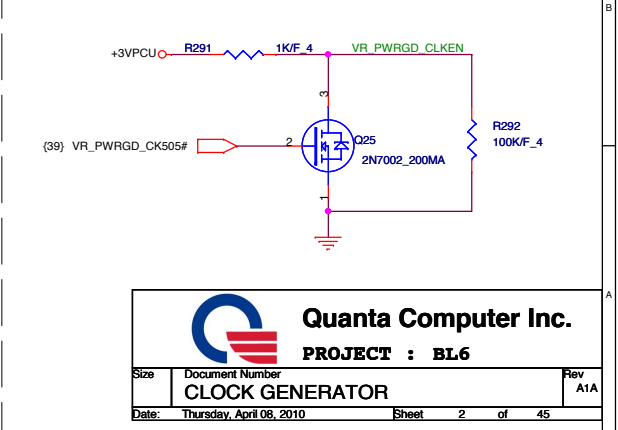
CLK CPU\_SEL

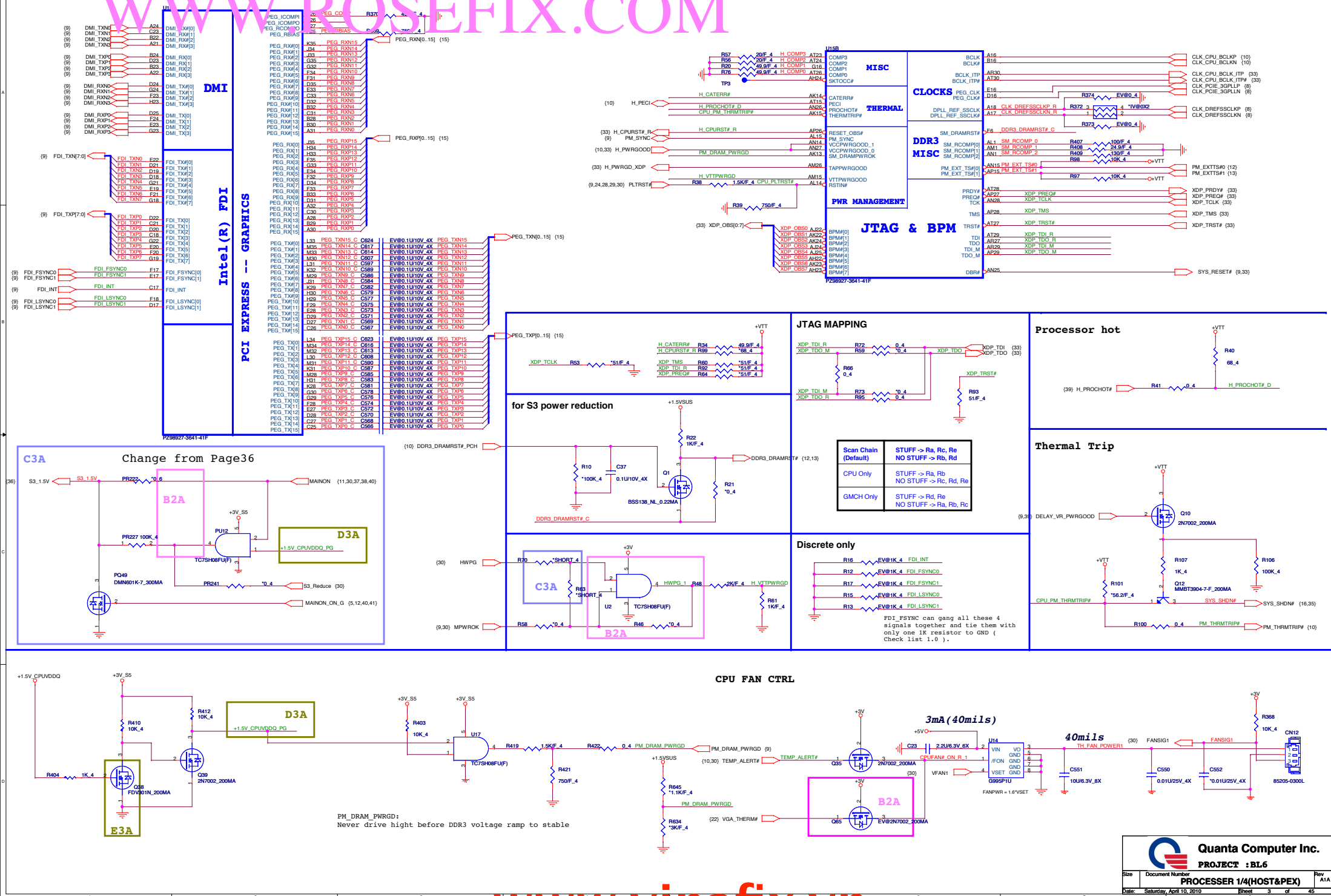


CLK I2C

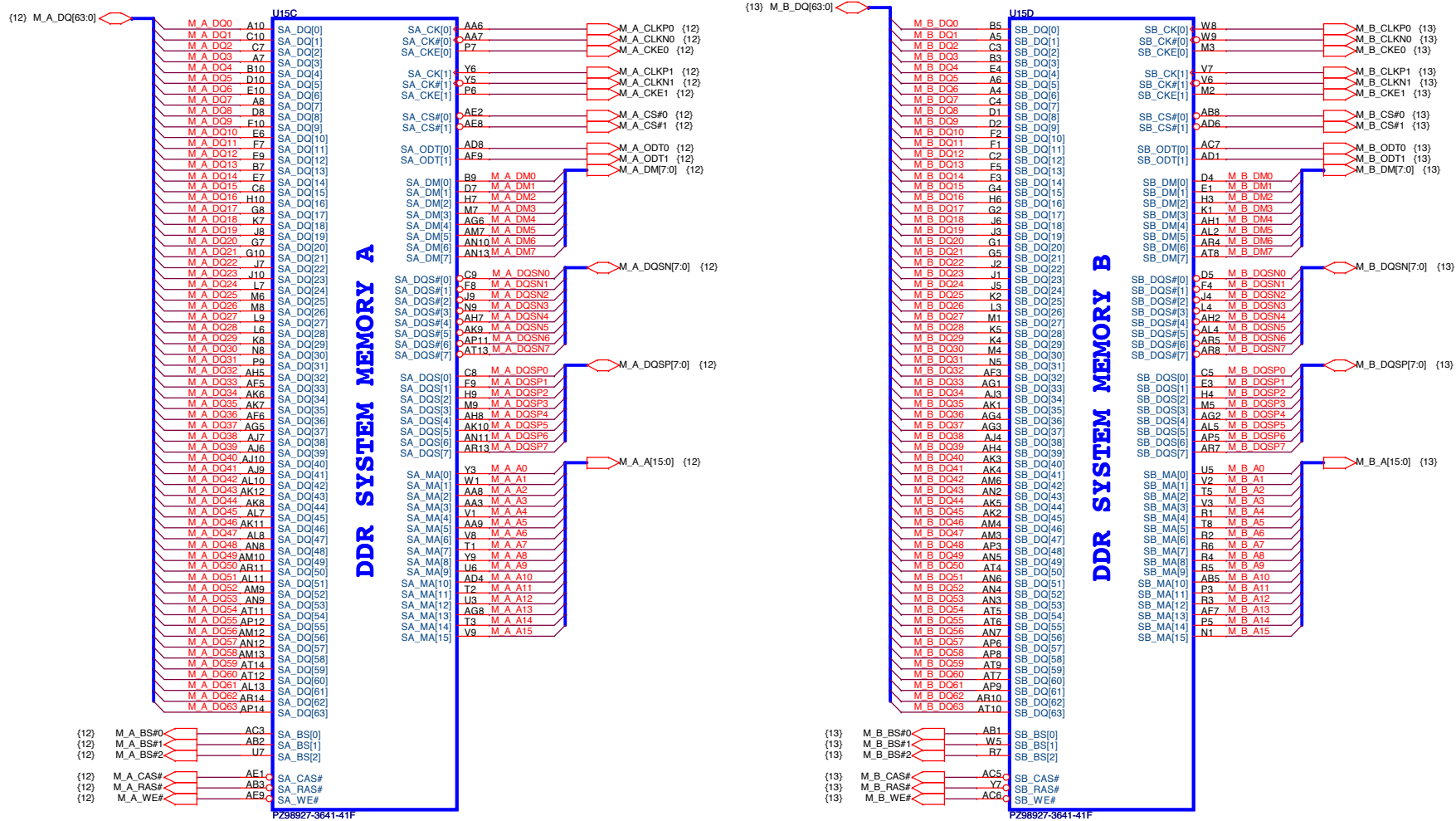


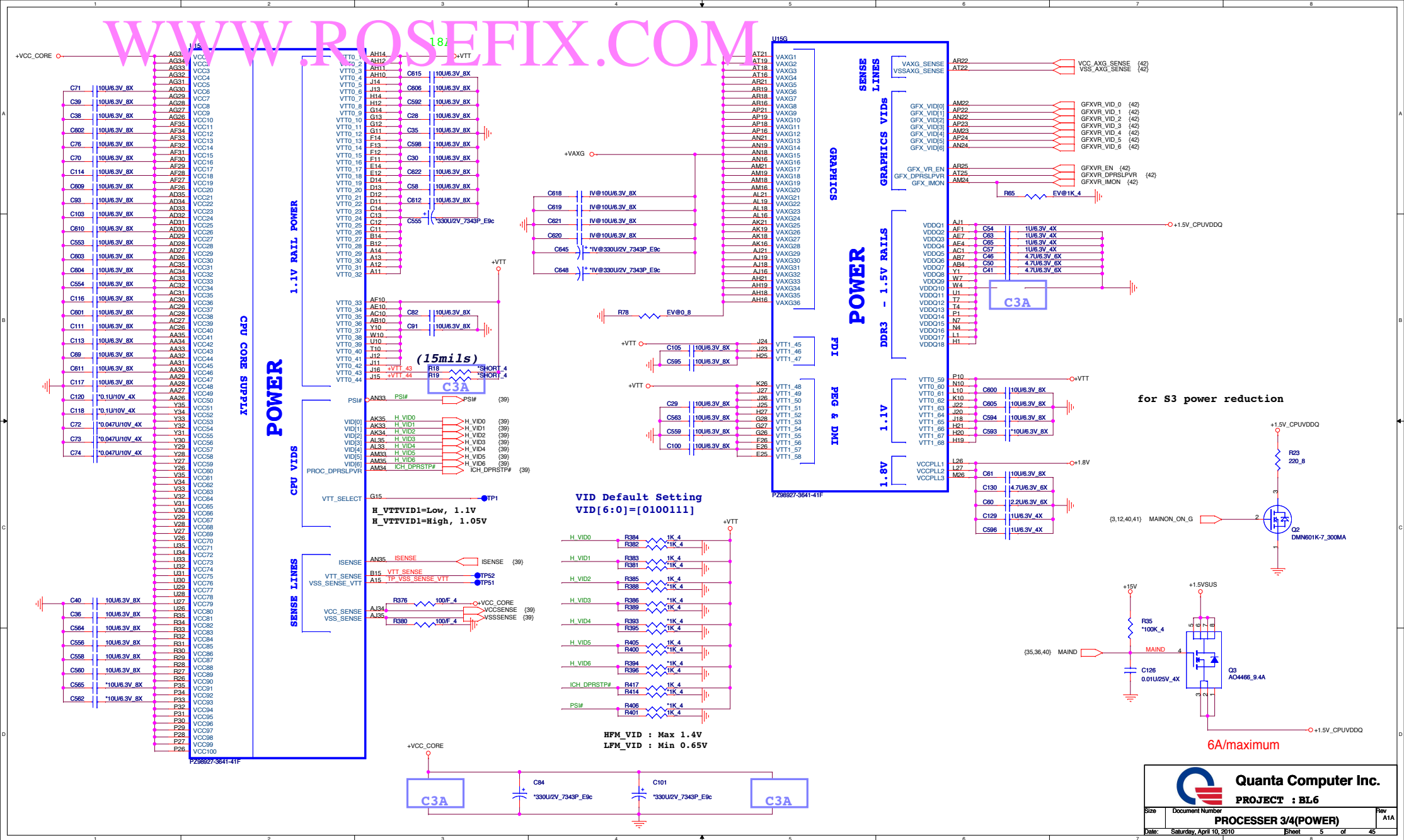
CLK POWERGOOD  
Change to +3VPCU  
(follow CRB)

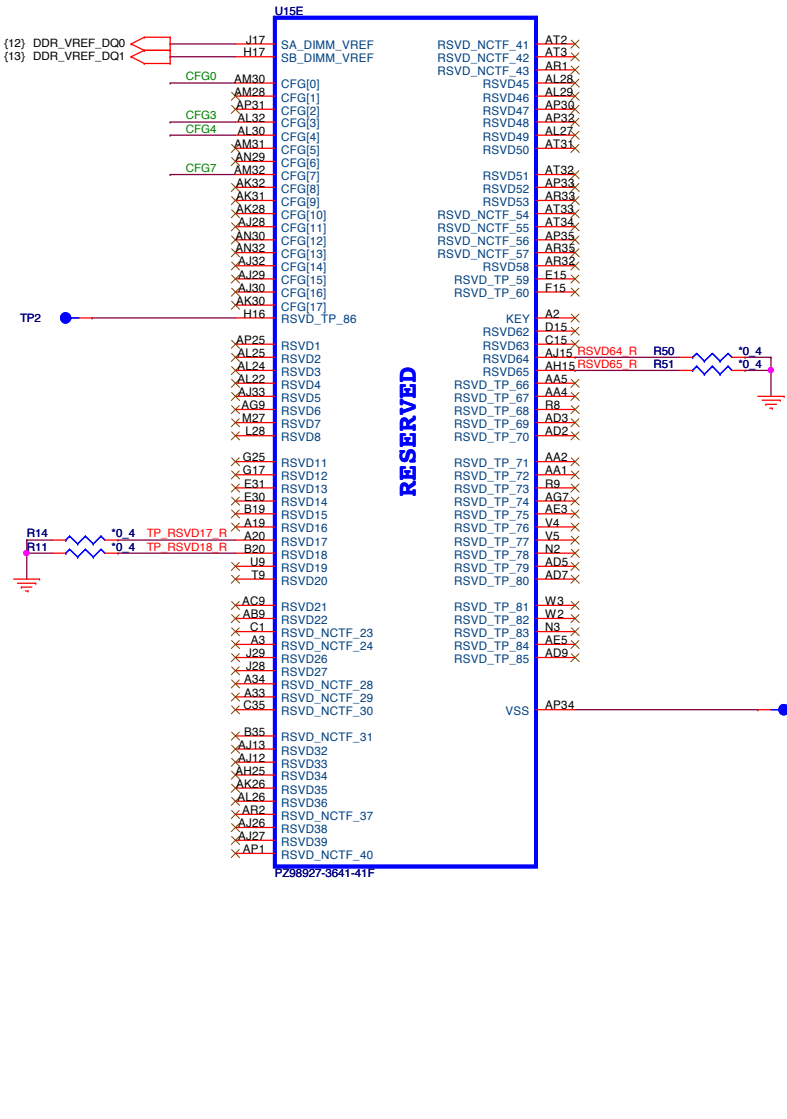
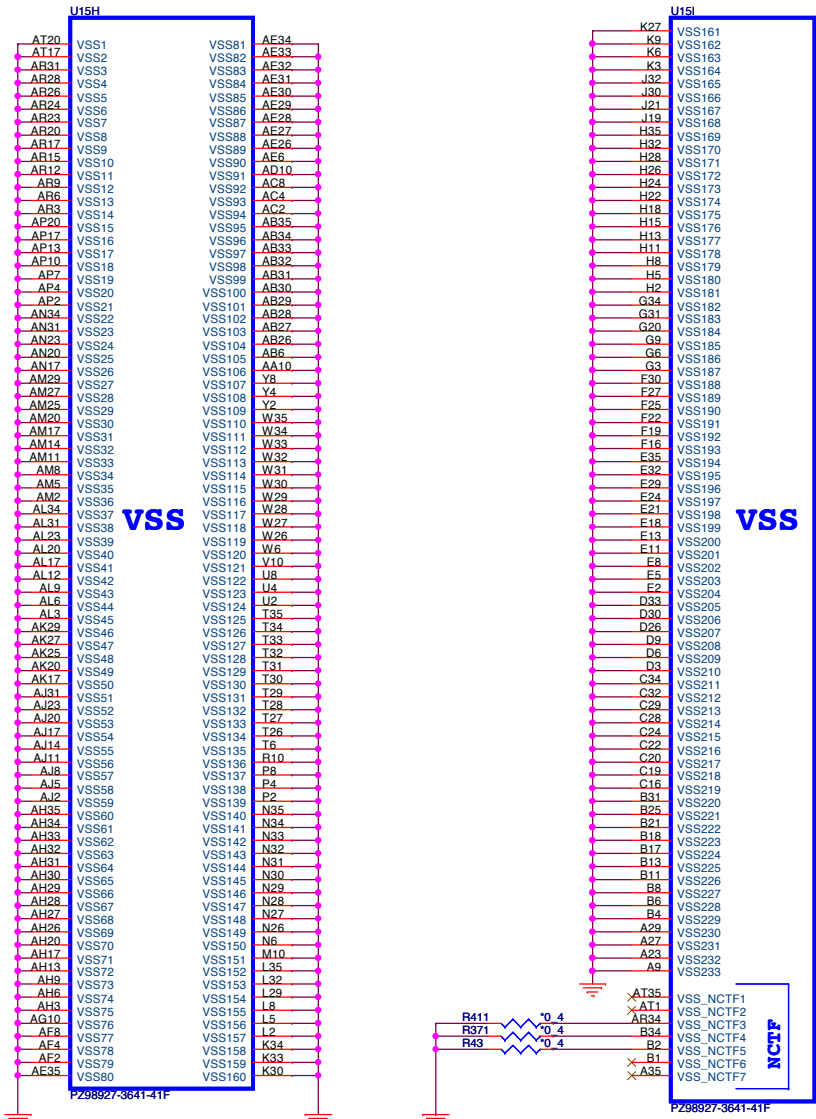




## AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

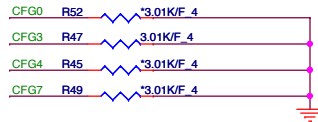






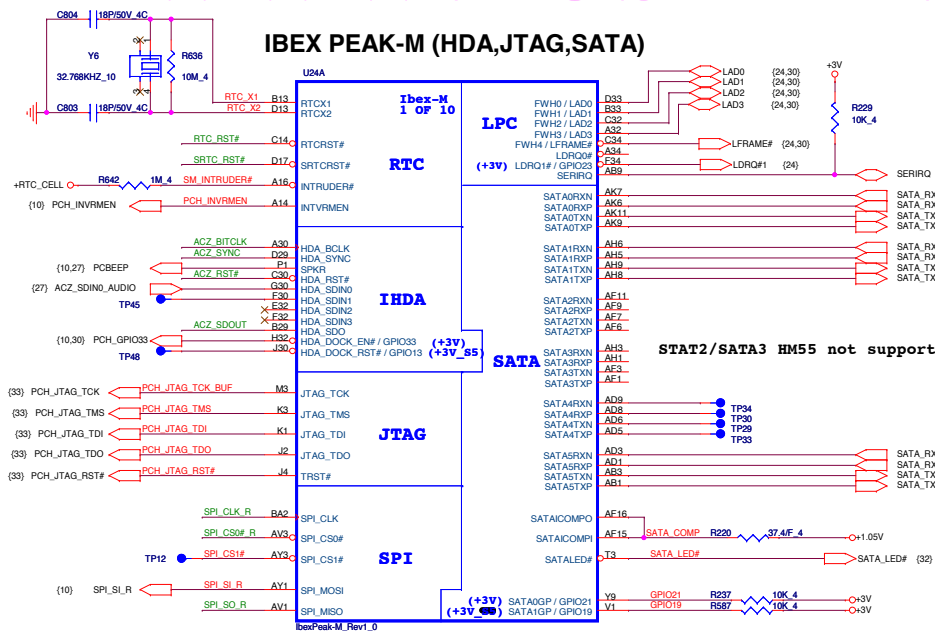
Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

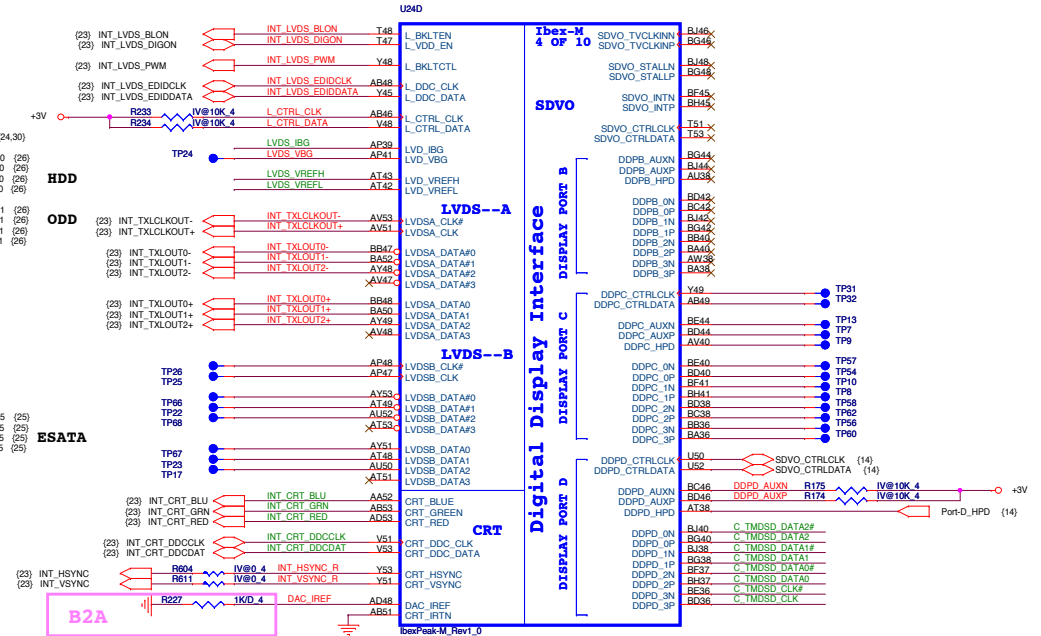




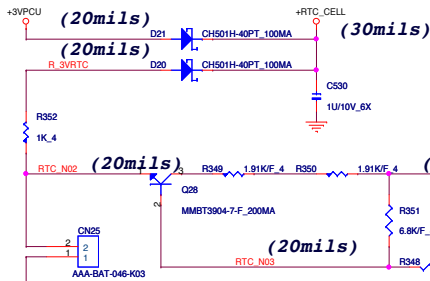
# IBEX PEAK-M (HDA,JTAG,SATA)



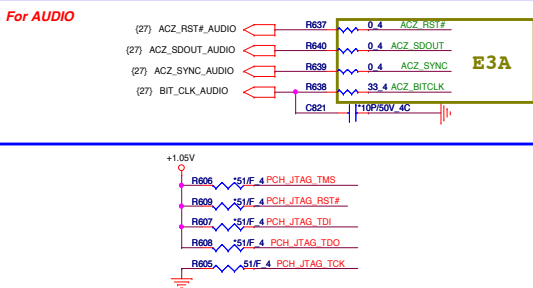
# IBEX PEAK-M (LVDS,DDI)



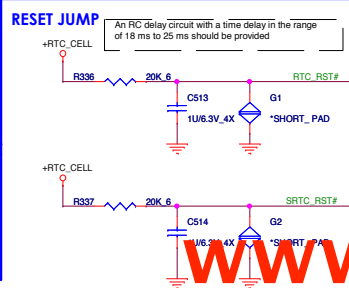
## RTC BATTERY



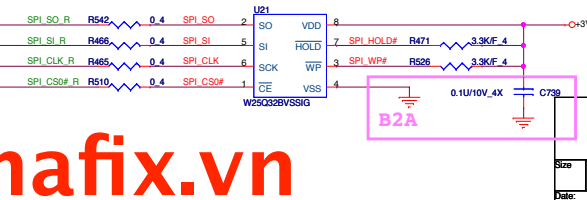
## For AUDIO



## RESET JUMP

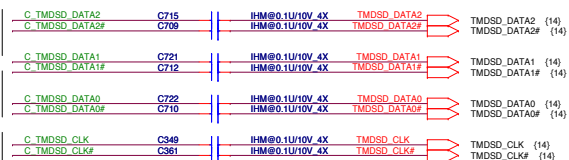


## 4M byte SPI ROM



Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC

## HDMI



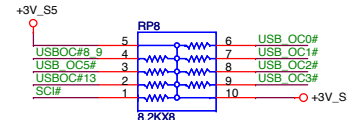
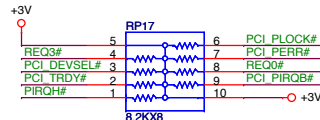
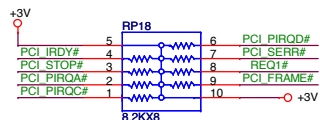
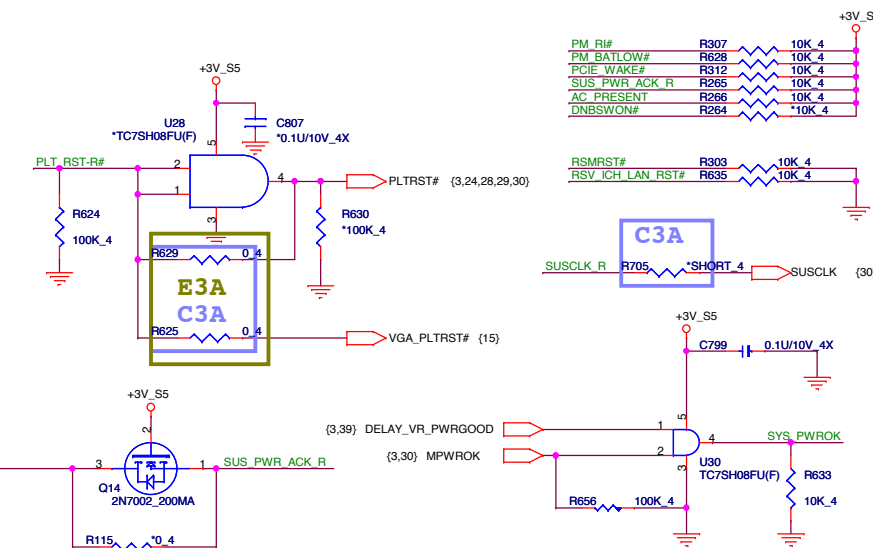
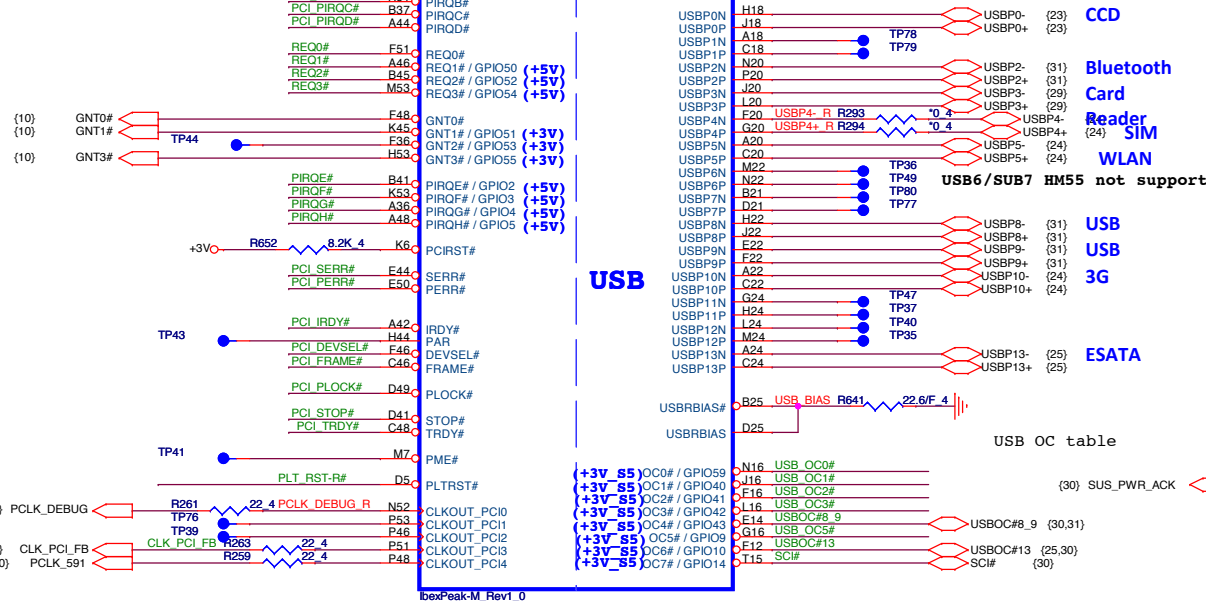
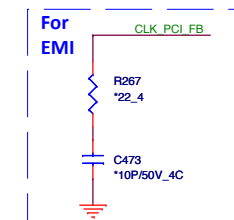
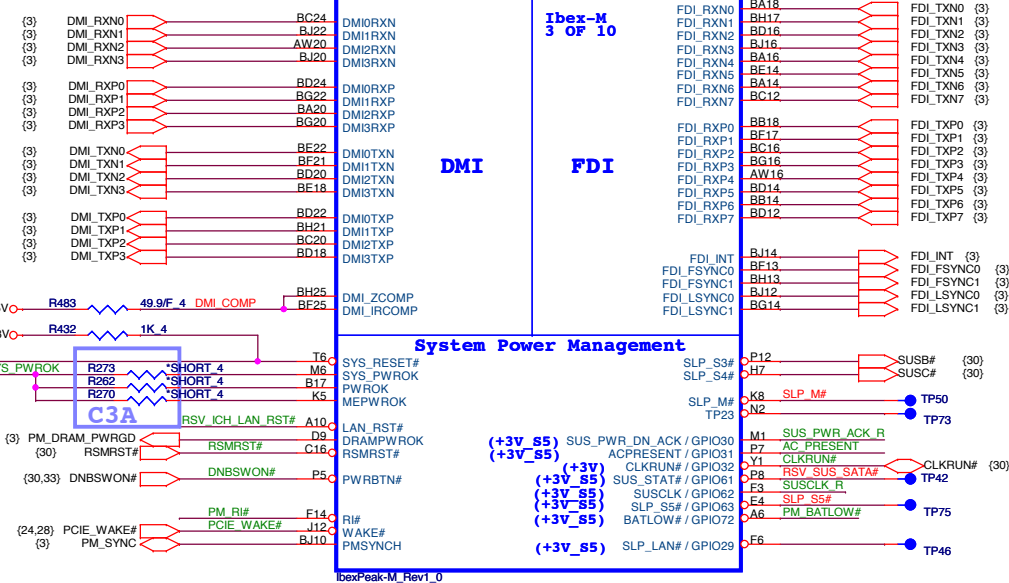
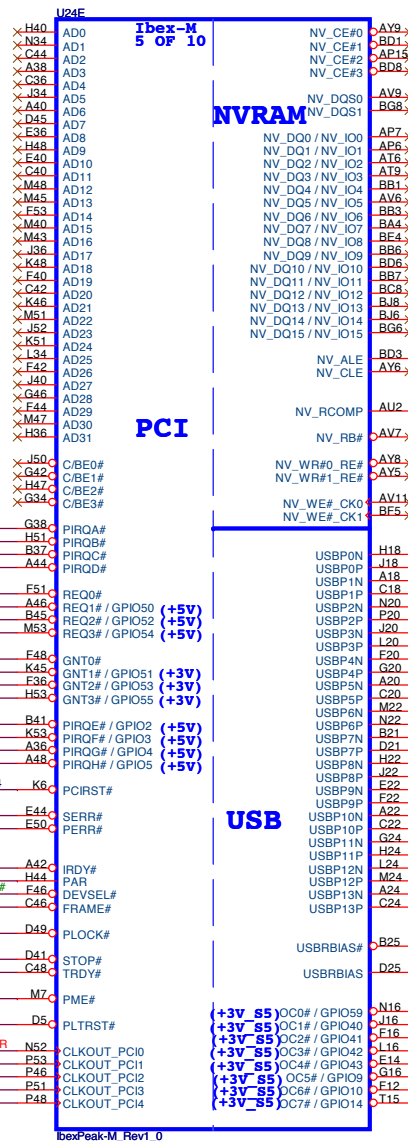
PCH	2MB	4MB	8MB
PM55	●		
HM55		●	
HM57/PM57		●	●
QM57/QS57			●

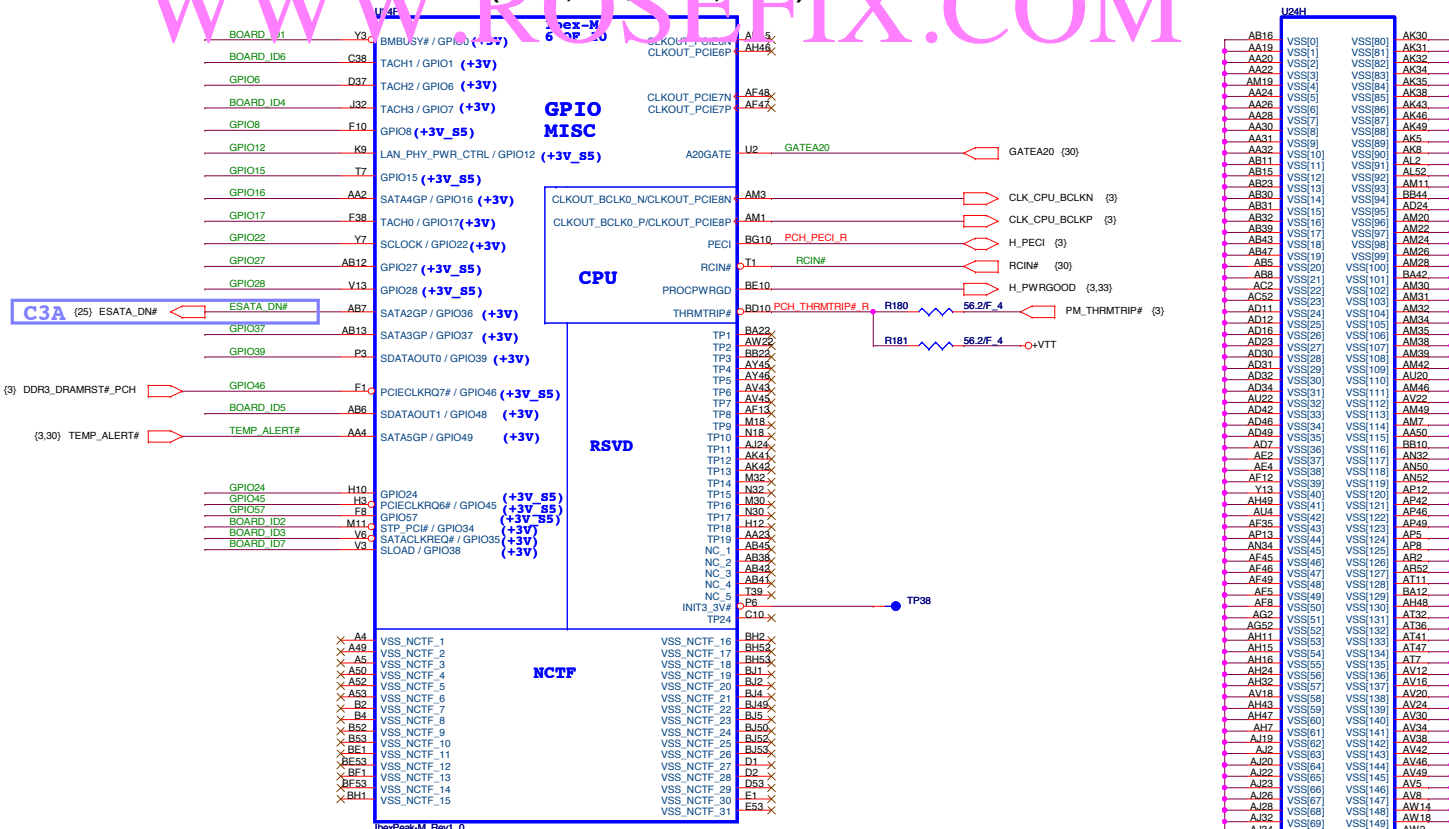




## IBEX PEAK-M (DMI,FDI,GPIO)

## IBEX PEAK-M (PCI,USB,NVRAM)





**SPKR**

(7,27) PCBEEP R592 \*1K\_4 +3V

Reboot option at power-up  
0 = Default Mode (Internal weak Pull-down)  
1 = No Reboot Mode with TCO Disabled

---

**GNT3# / GPIO55**

(9) GNT3# R622 \*10K\_4

Top-Block Swap Override  
0 = Top Block Swap Mode  
1 = Default Mode (Internal pull-up)

---

**HDA\_DOCK\_EN #GPIO33**

(7,30) PCH\_GPIO33 R282 \*1K\_4 JP1 \*SHORT PAD

Flash Descriptor Security Override  
0 = Flash Descriptor Security will be overridden  
1 = Security measure defined in the Flash Descriptor will be enabled.

---

**GNT0#, GNT1#**

(9) GNT0# R272 \*1K\_4  
(9) GNT1# R621 \*1K\_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI

---

**SPI\_MOSI**

(7) SPI\_SI\_R R504 \*1K\_4 +3V

TPM Functionality Disable  
1 = Enabled  
0 = Disable

---

**NV\_ALE**

(9) NV\_ALE R496 \*10K\_4 +1.8V

IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable  
1 = Enabled  
0 = Disabled (Default)

---

**GPIO8**

GPIO8 R298 \*10K\_4 +3V\_S5

Reserved  
This signal has a weak internal pull up.  
NOTE: This signal should not be pulled low

---

**GPIO15**

GPIO15 R248 \*1K\_4 +3V\_S5

Reserved  
0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality  
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

---

**GPIO27**

GPIO27 R232 \*10K\_4

On-Die PLL Voltage Regulator  
0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails.  
1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. This signal has a weak internal pull-up.

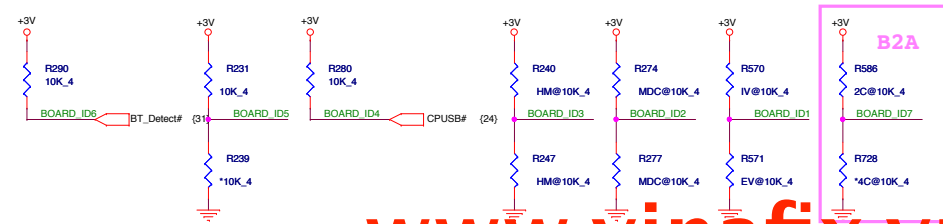
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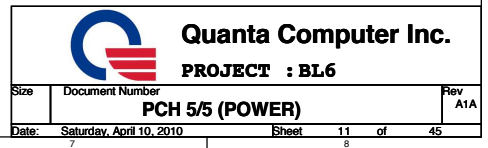
+RTC\_CELL R644 \*330K\_6 PCH\_INVRMEN PCH\_INVRMEN (7)

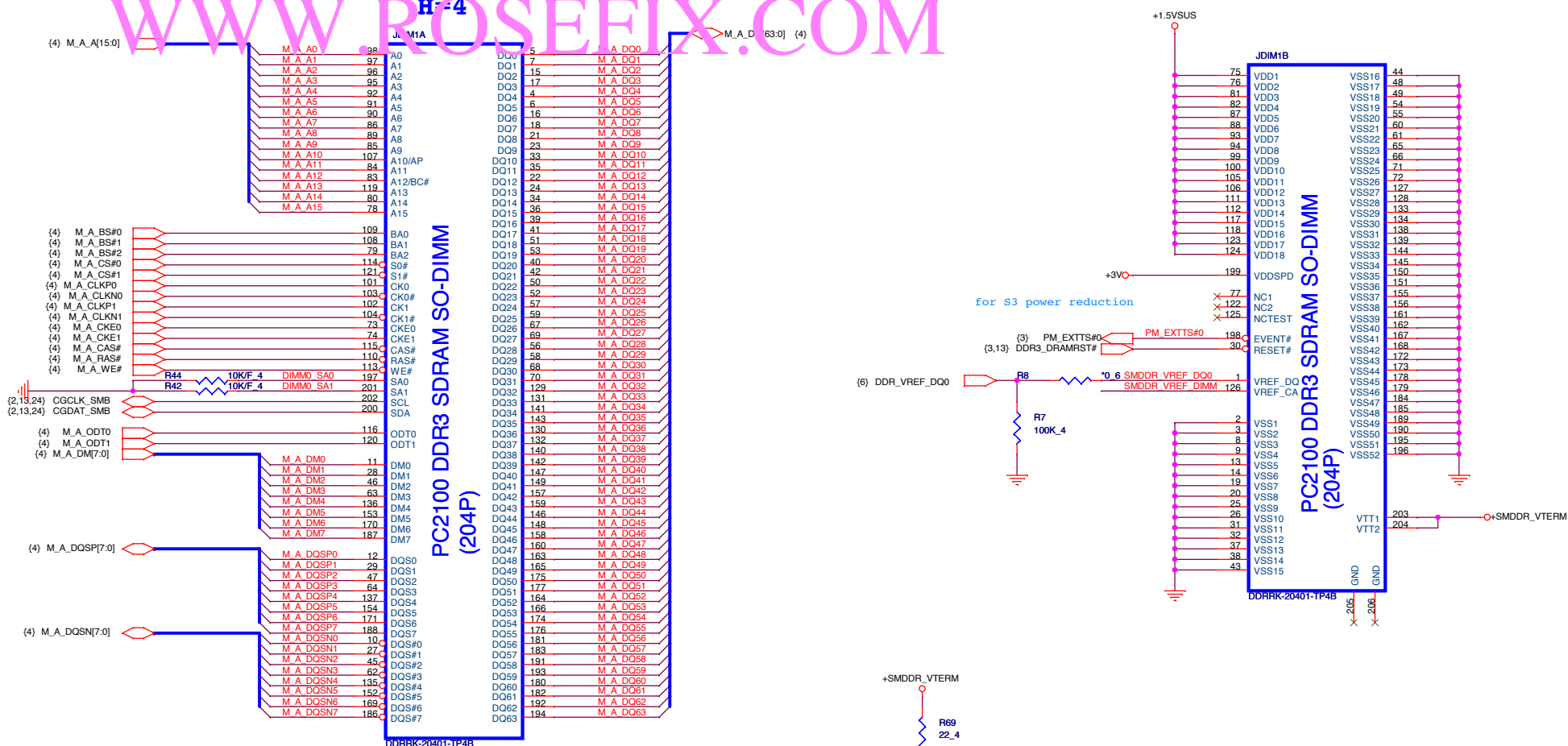
INTVRMEN - Integrated SUS 1.1V VRM Enable  
High - Enable Internal VRs

BOARD ID SETTING

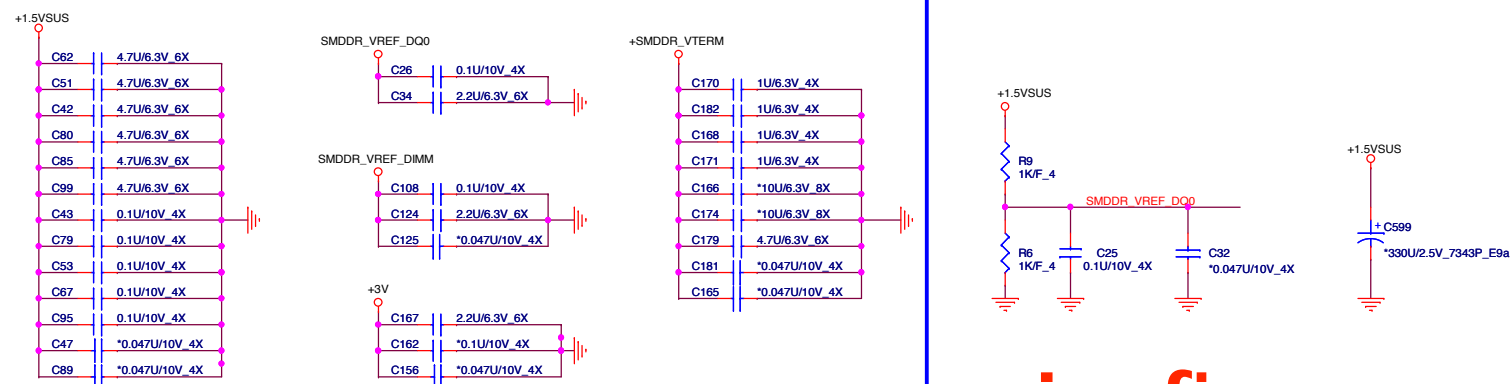
Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7
UMA SKU VGA SKU	H	L					
W/ MDC W/O MDC			H	L			
W/ HDMI W/O HDMI			H	L			
W/O 3G W/ 3G				H	L		
15" 14"					H	L	
W/O BT W/ BT						H	L
2 Core 4 Core							H



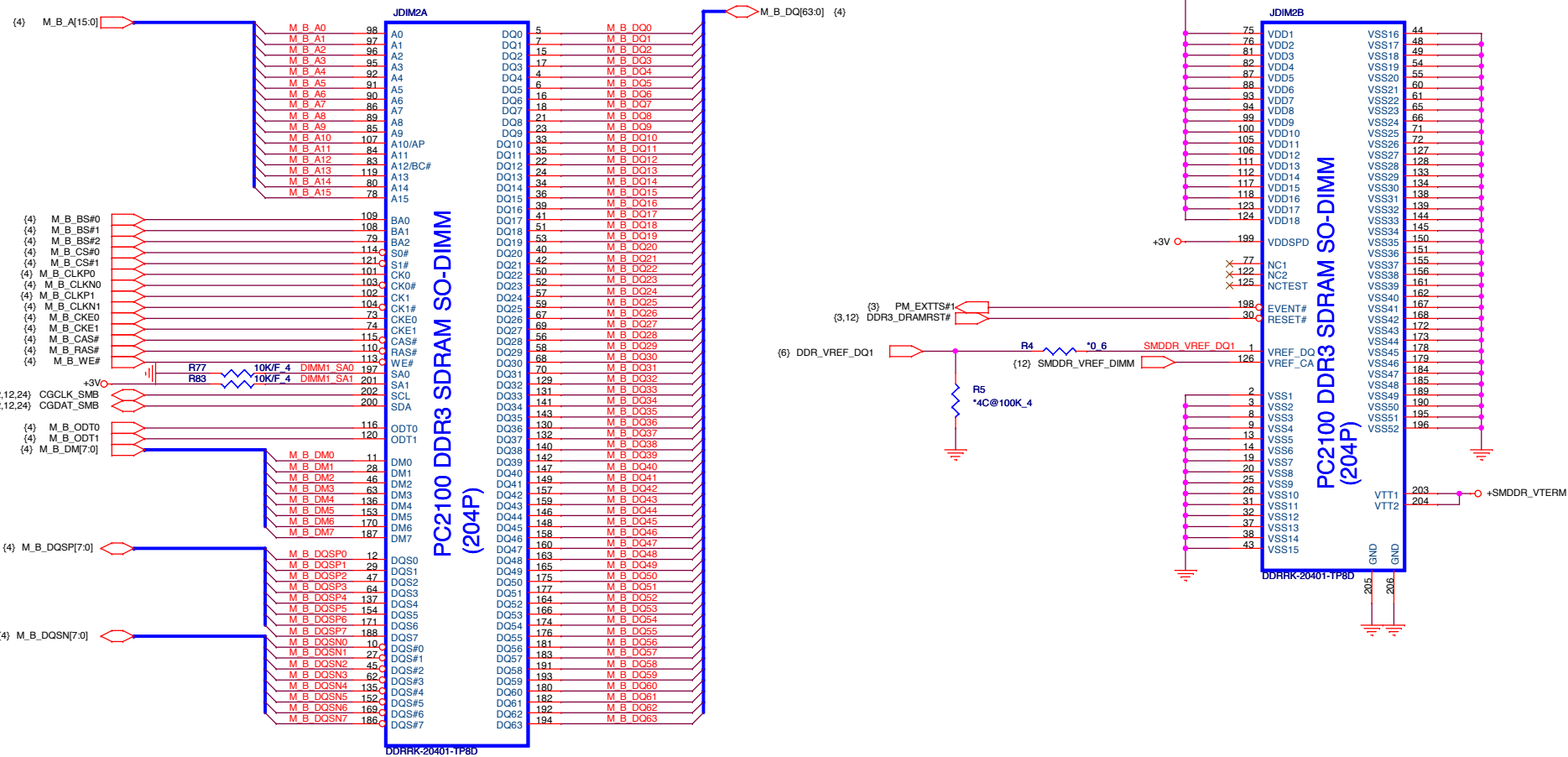




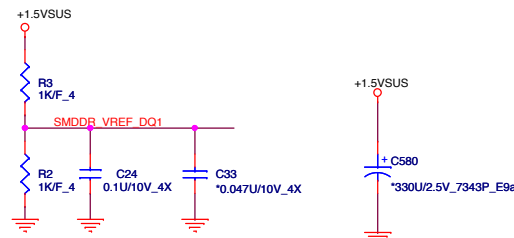
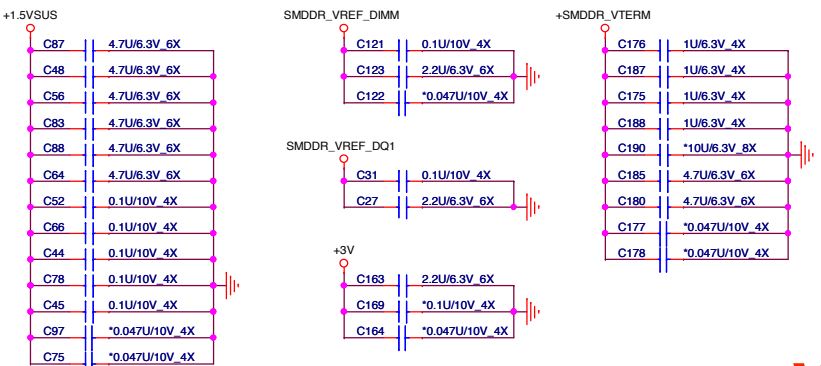
***Place these Caps near So-Dimm0.***



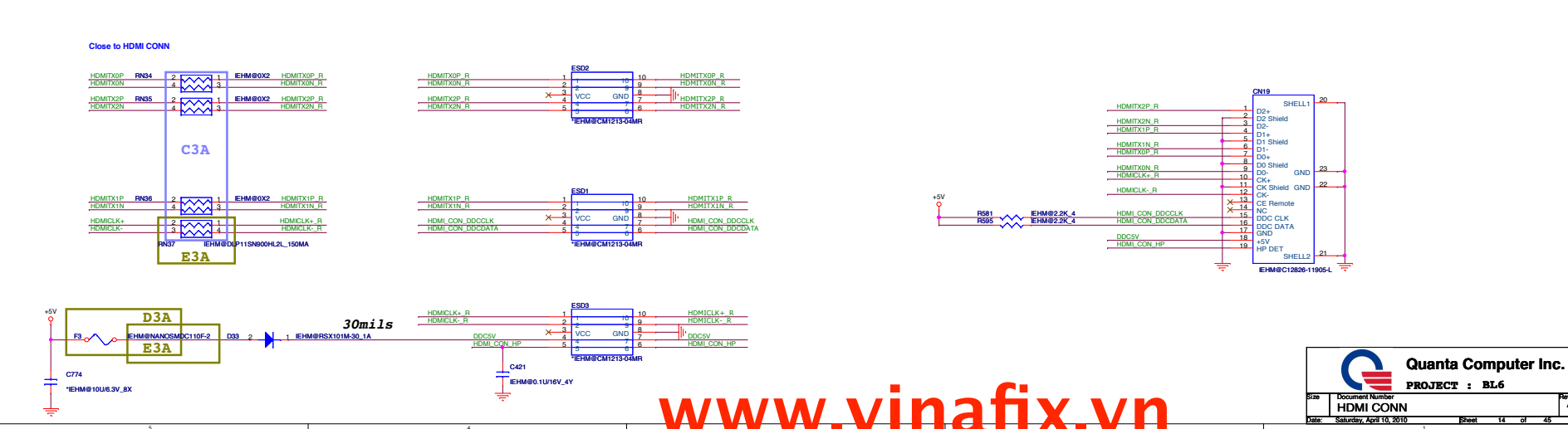
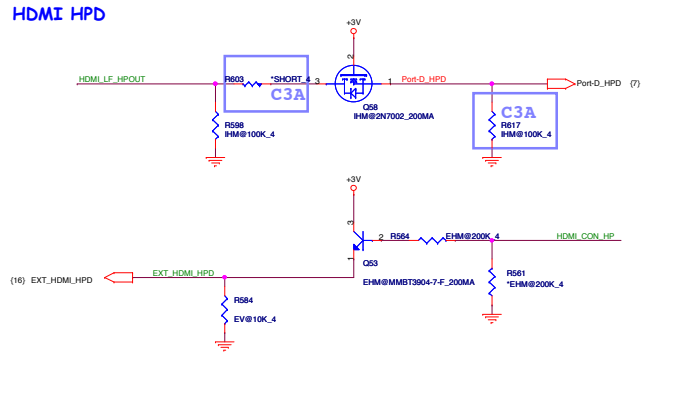
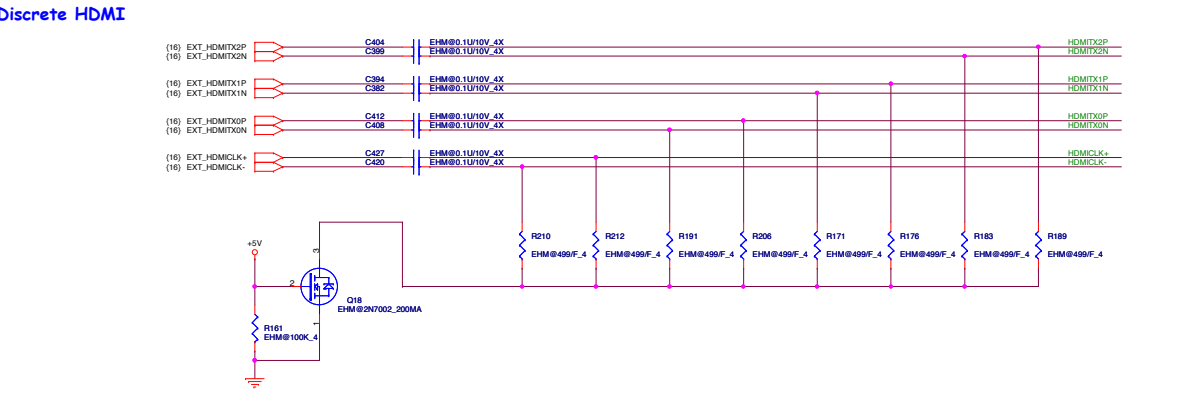
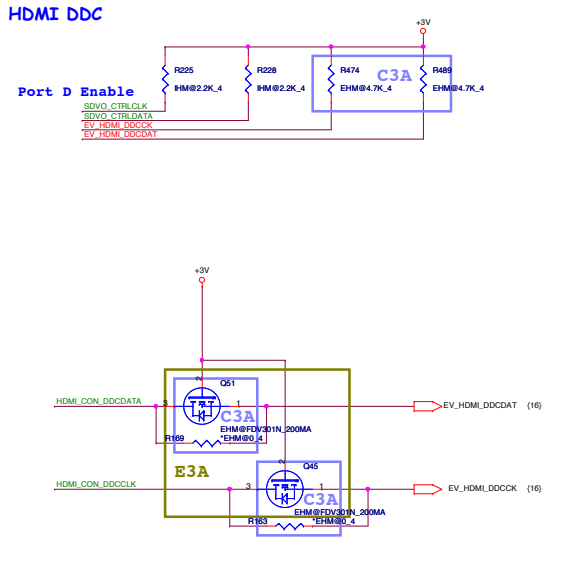
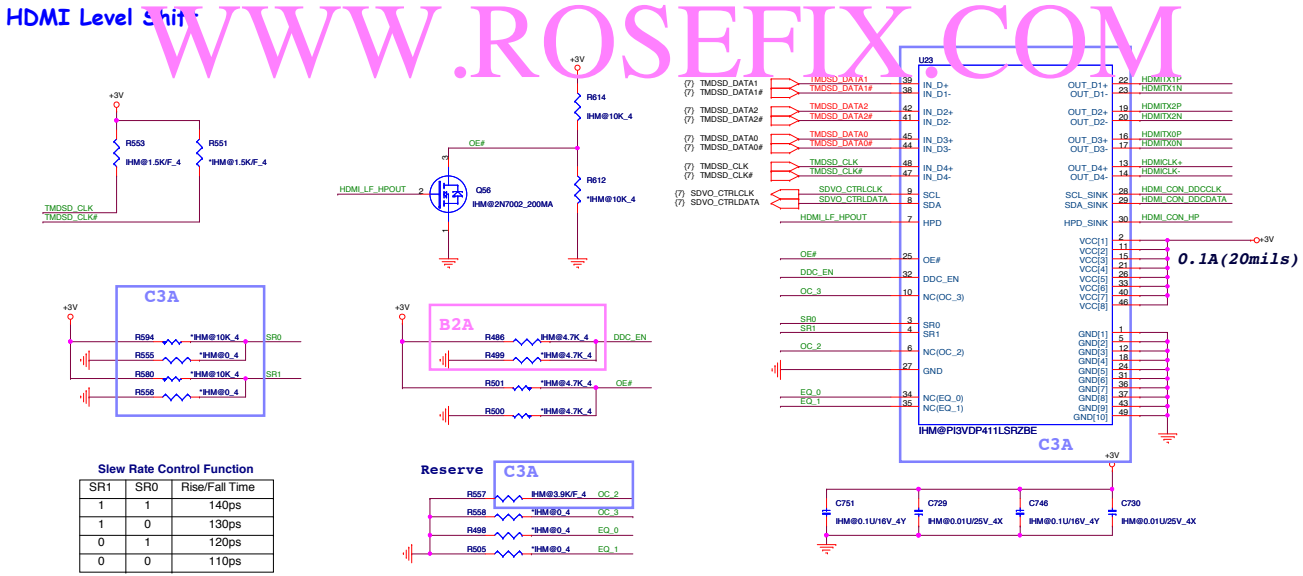


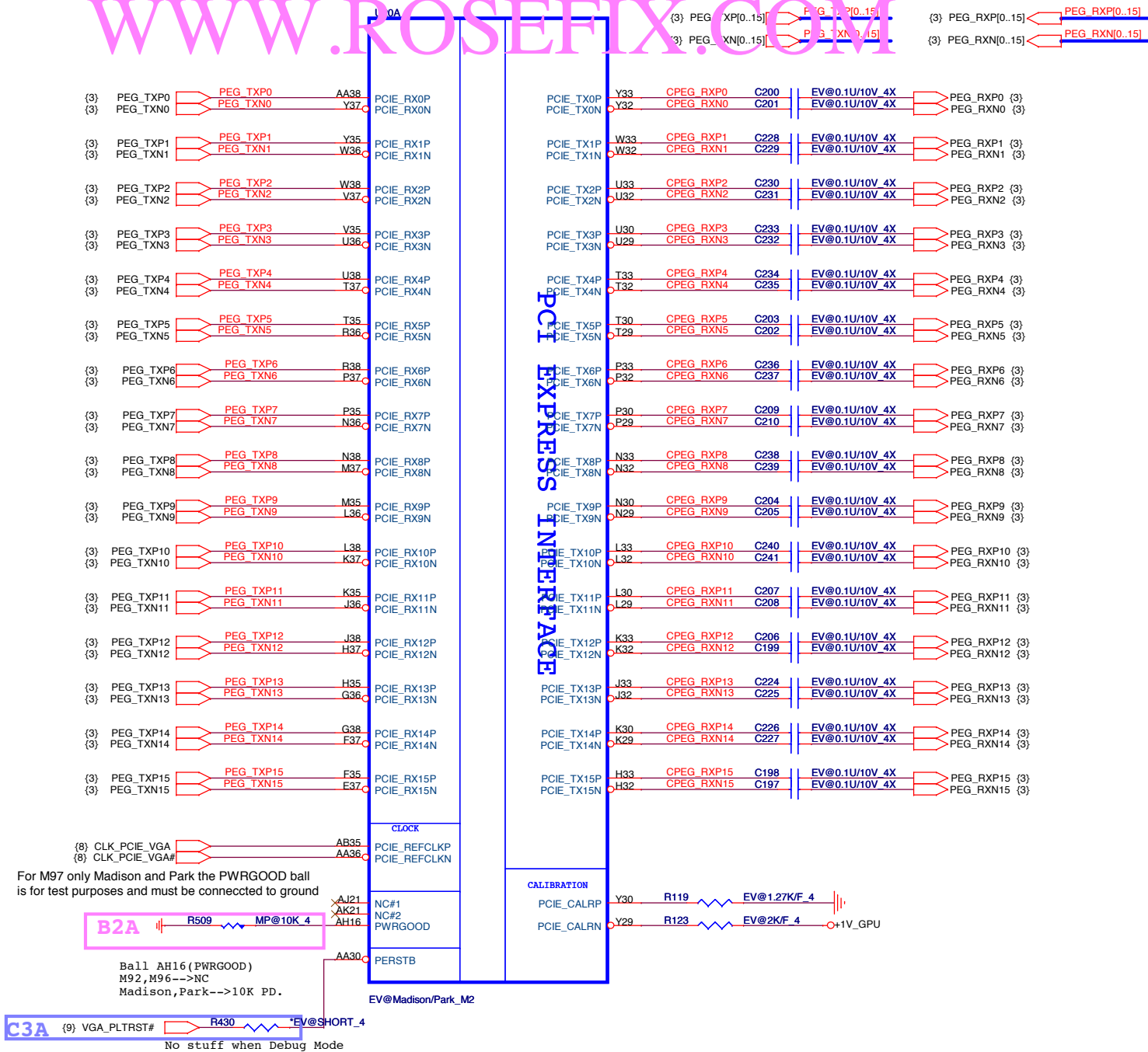


Place these Caps near So-Dimm1.

















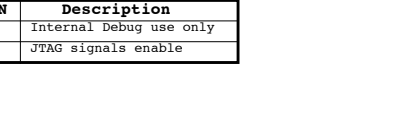
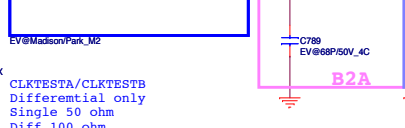
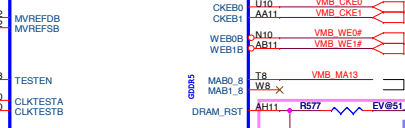
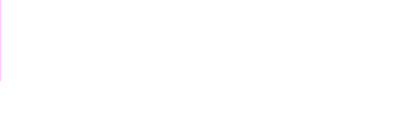
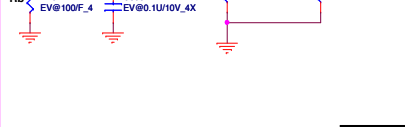
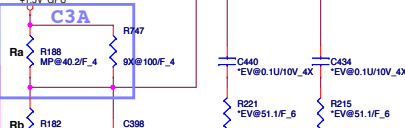
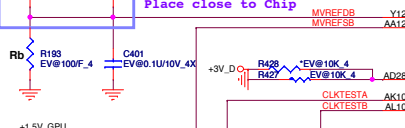
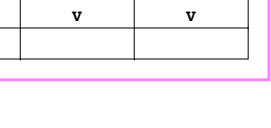
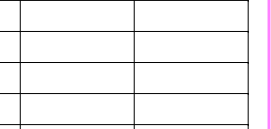
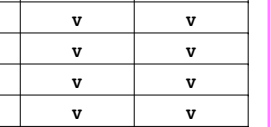
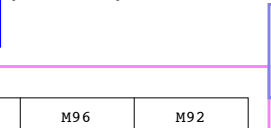
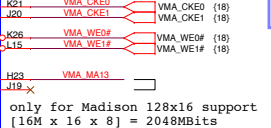
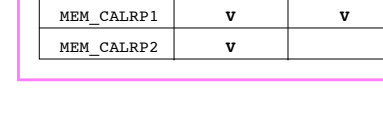
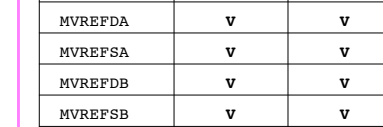
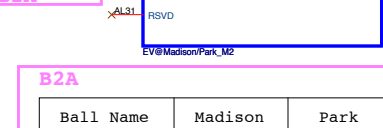
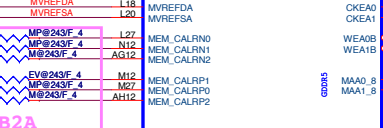
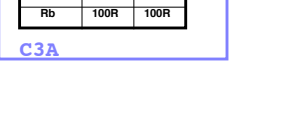
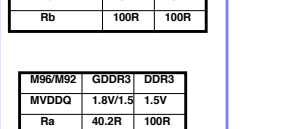
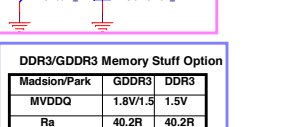
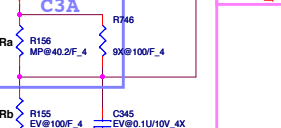
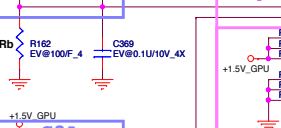
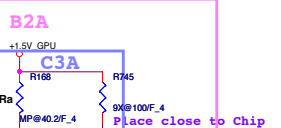
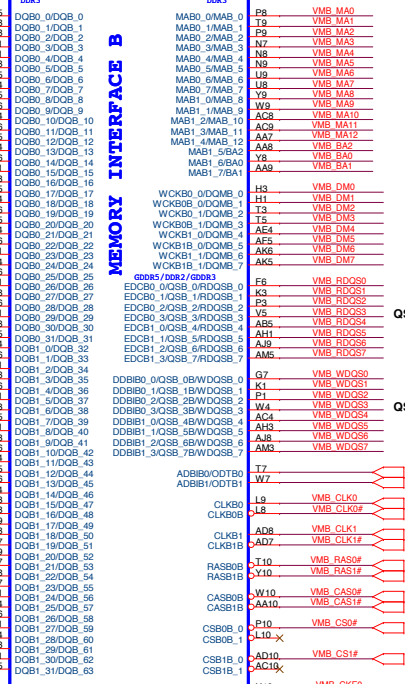
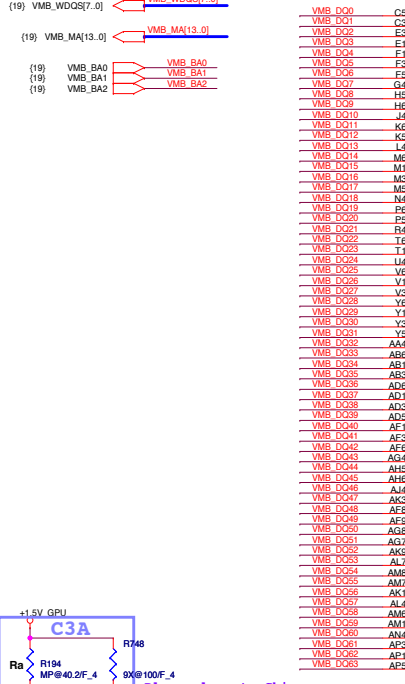
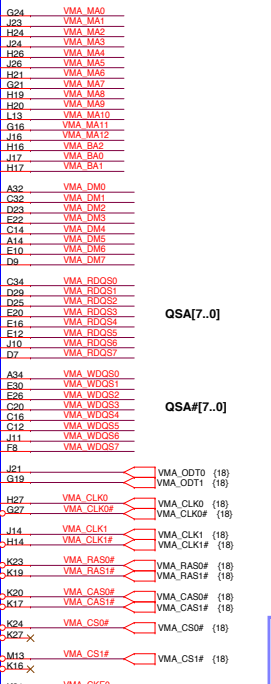
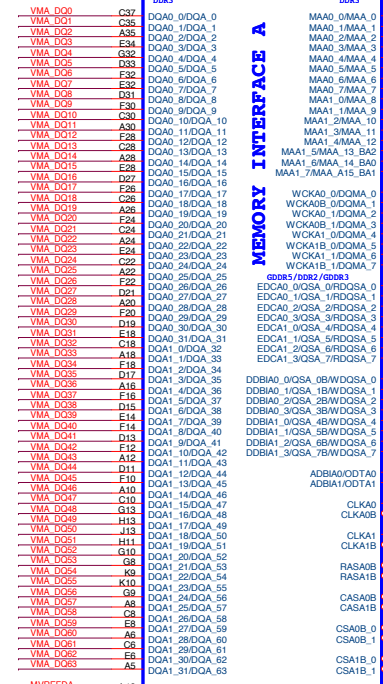


(18) VMA\_DQ[63..0]  VMA\_DQ[63..0]  
(18) VMA\_DM[7..0]  VMA\_DM[7..0]  
(18) VMA\_RQS[7..0]  VMA\_RQS[7..0]  
(18) VMA\_WQS[7..0]  VMA\_WQS[7..0]

(18) VMA\_MA[13..0]  VMA\_MA[13..0]  
(18) VMA\_BA0  VMA\_BA0  
(18) VMA\_BA1  VMA\_BA1  
(18) VMA\_BA2  VMA\_BA2

(19) VMB\_DQ[63..0]  VMB\_DQ[63..0]  
(19) VMB\_DM[7..0]  VMB\_DM[7..0]  
(19) VMB\_RQS[7..0]  VMB\_RQS[7..0]  
(19) VMB\_WQS[7..0]  VMB\_WQS[7..0]

(19) VMB\_MA[13..0]  VMB\_MA[13..0]  
(19) VMB\_BA0  VMB\_BA0  
(19) VMB\_BA1  VMB\_BA1  
(19) VMB\_BA2  VMB\_BA2



Ball Name	Madison	Park	M96	M92
MVREFDA	V	V	V	V
MVREFSA	V	V	V	V
MVREFDB	V	V	V	V
MVREFSB	V	V	V	V
MEM_CALRN0	V	V	V	V
MEM_CALRN1	V	V	V	V
MEM_CALRN2	V	V	V	V
MEM_CALRP0	V	V	V	V
MEM_CALRP1	V	V	V	V
MEM_CALRP2	V	V	V	V

Madison/Park	DDR3	DDR3
MVDDQ	1.8V/1.5	1.5V
Ra	40.2R	40.2R
Rb	100R	100R

M96/M92	DDR3	DDR3
MVDDQ	1.8V/1.5	1.5V
Ra	40.2R	100R
Rb	100R	100R

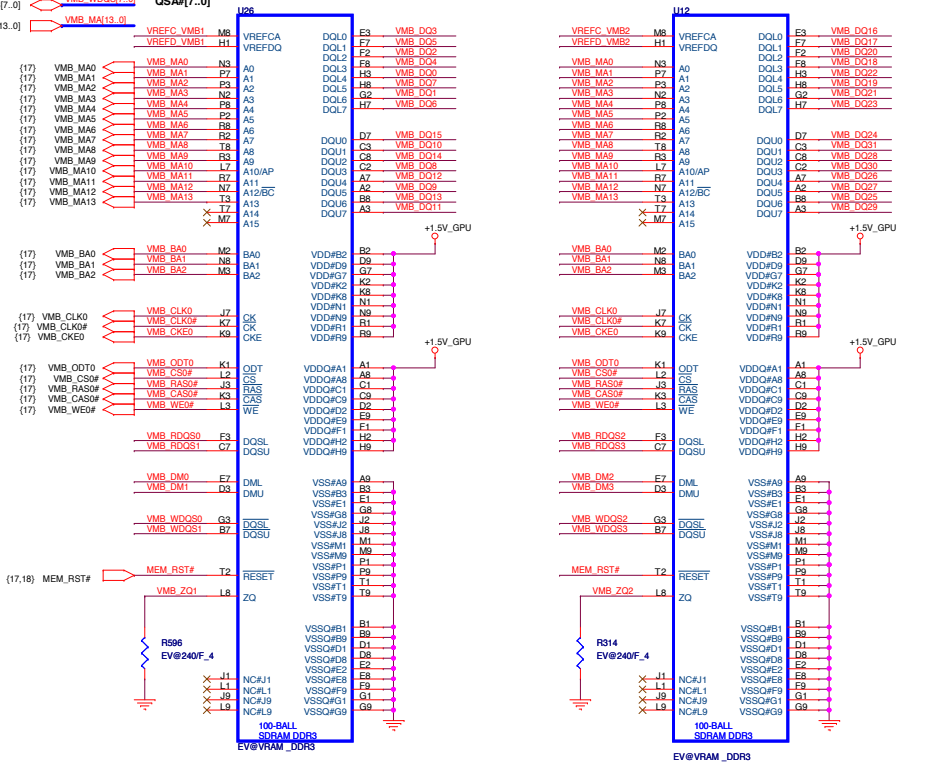
TESTEN	Description
0	Internal Debug use only
1	JTAG signals enable



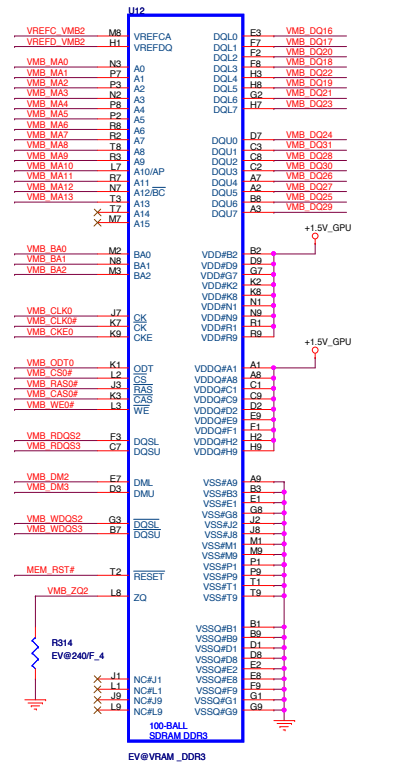


(17) VMB\_DQ[63..0]  
(17) VMB\_DM[7..0]  
(17) VMB\_RDQS[7..0]  
(17) VMB\_WDQS[7..0]  
(17) VMB\_MA[13..0]

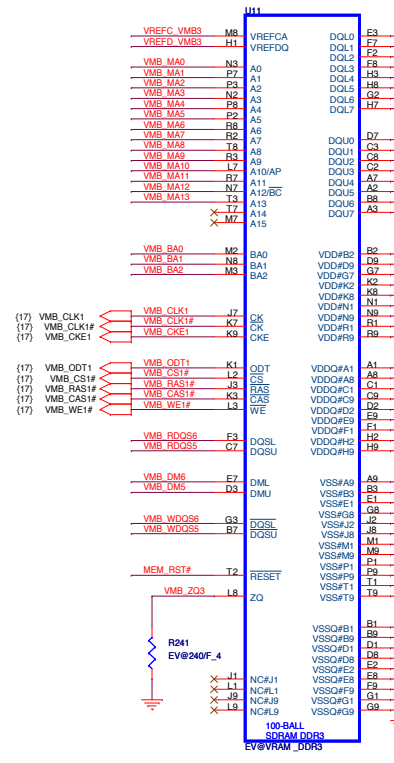
QSA[7..0]  
QSA#[7..0]



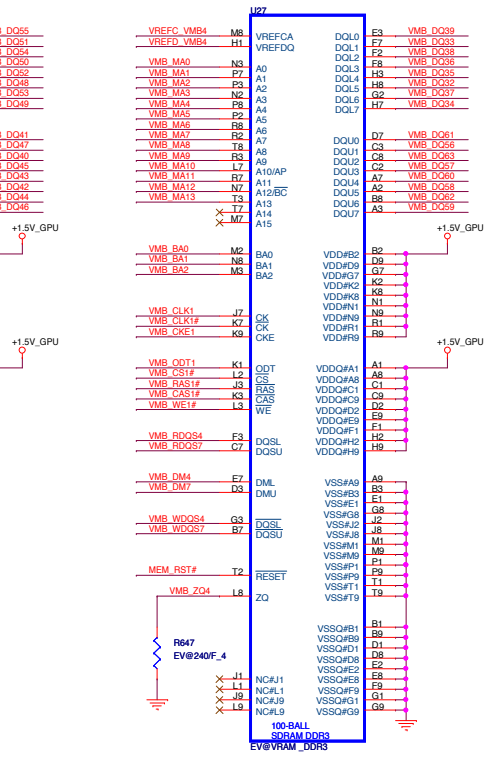
BOT Down



TOP Down

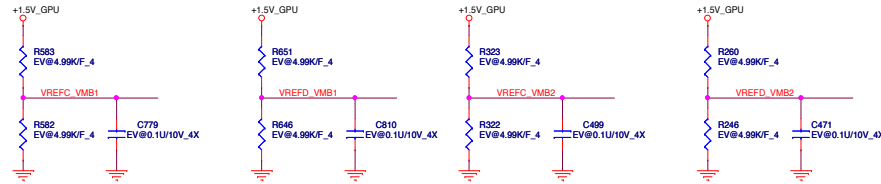


TOP Up

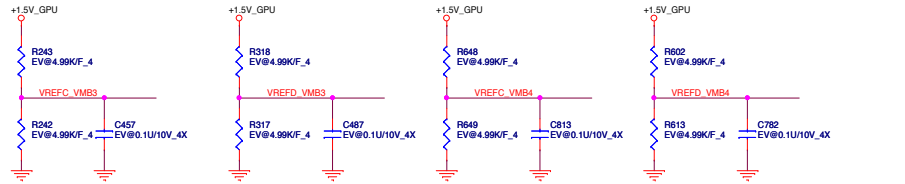


BOT Up

## Group-B0 VREF

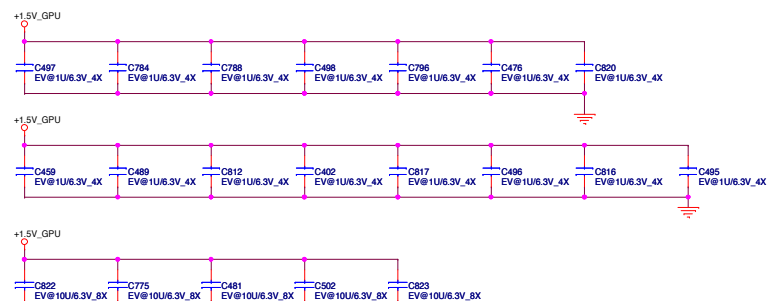


## Group-B1 VREF

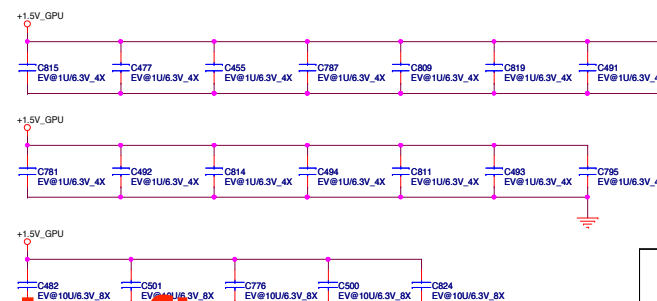


## MEM\_B0 CLK

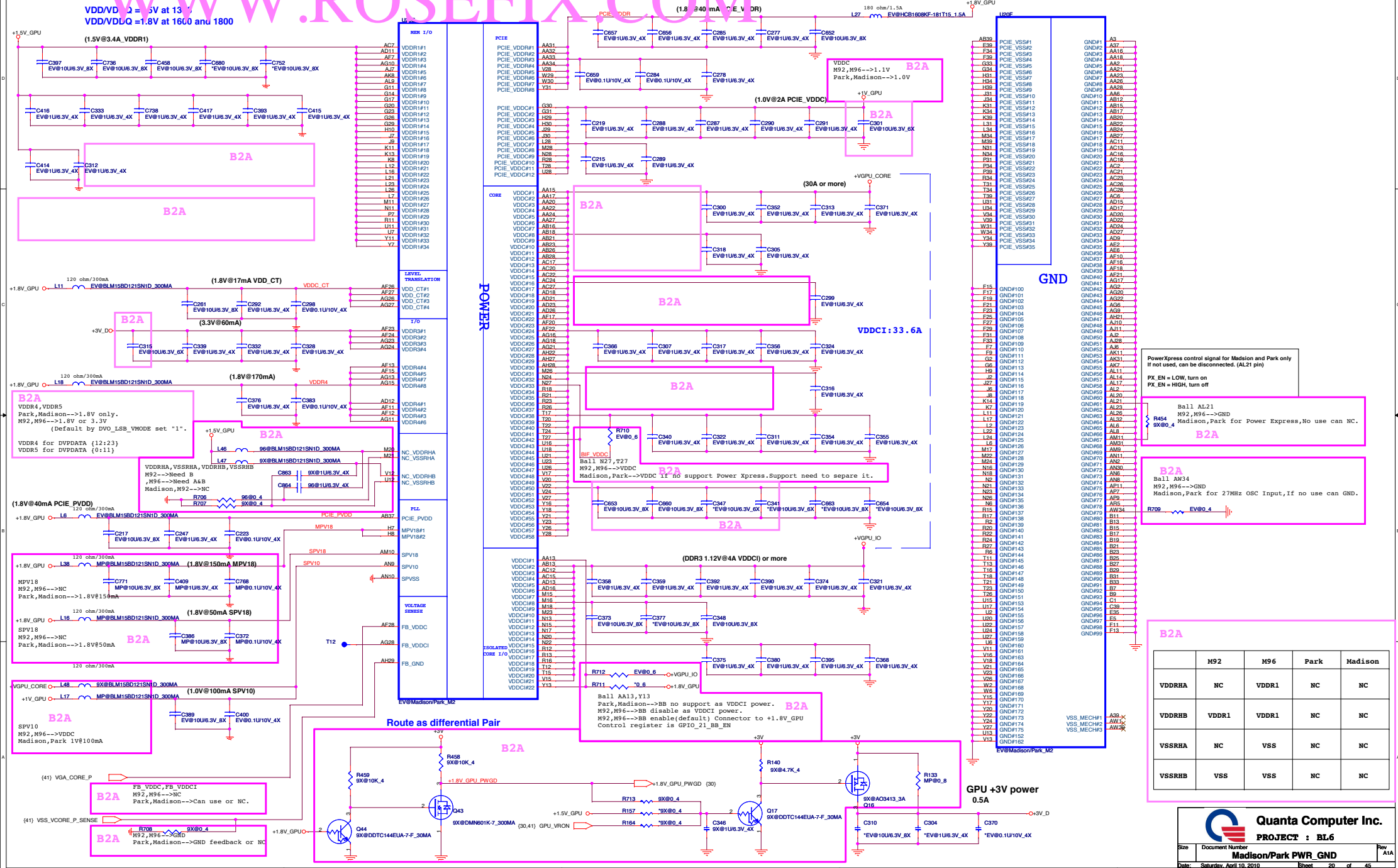
## Group-B0 decoupling CAP



## Group-B1 decoupling CAP

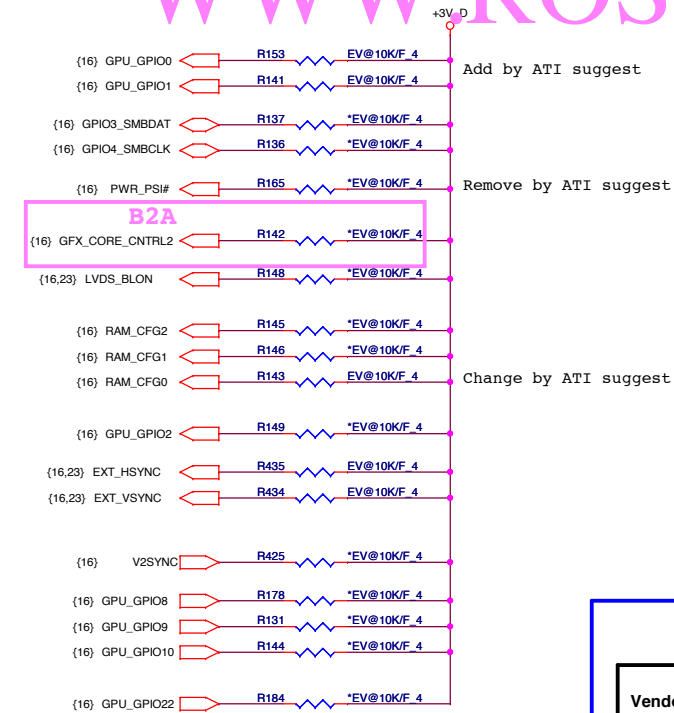


## MEM\_B1 CLK





## PIN STRAPS



Memory Aperture size	
RAM_CFG[2:0]	Size
000	128MB
001	256MB
010	64MB
011	32MB

ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by detect
1	0	DP only
1	1	Both DP & HDMI

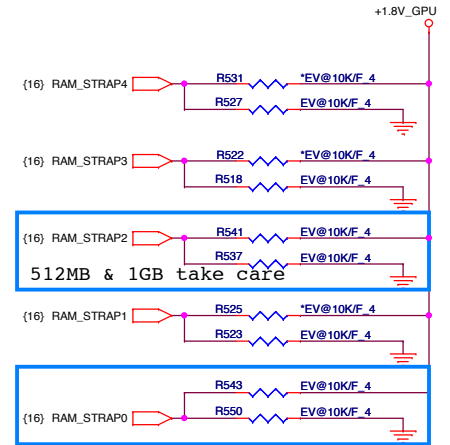
## CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

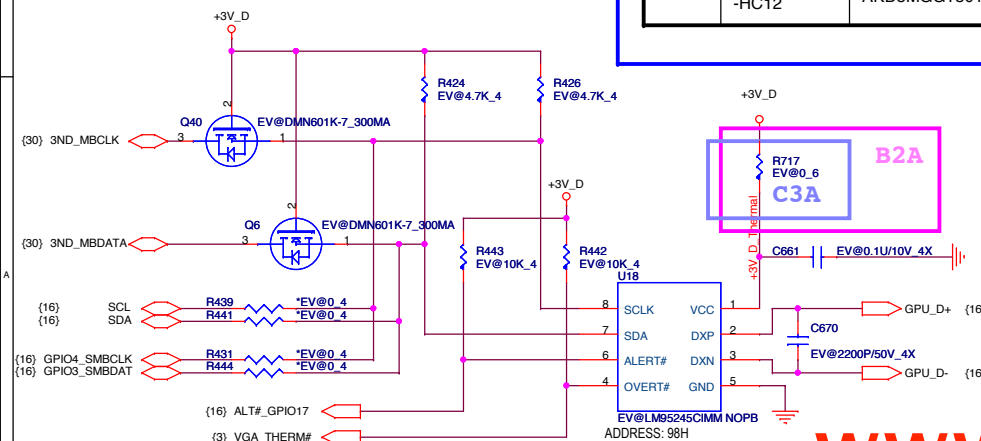
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

## DDR3 Memory TYPE

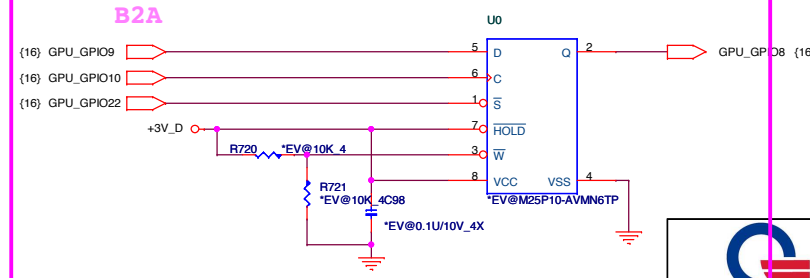
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	RAM_STRAP4	
								15"	14"
Hynix	H5TQ1G63BFF-12C	AKD5LZGTW00 (64M*16)	512MB	0	1	0	0	0	1
			1GB	0	0	0	0	0	1
			2GB	0	0	1	0	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT502 (64M*16)	512MB	0	1	0	1	0	1
			1GB	0	0	0	1	0	1
	K4W2G1646B-HC12	AKD5MGGT501	2GB	0	0	1	1	0	1



## Thermal Sensor



## EEPROM



Quanta Computer Inc.  
PROJECT : BL6



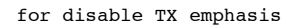




Pir 0/16/20

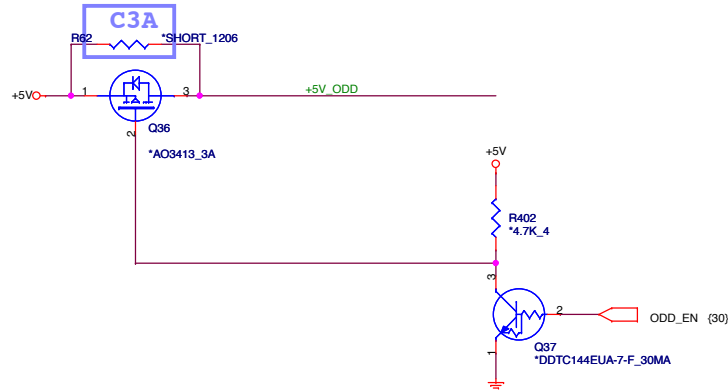
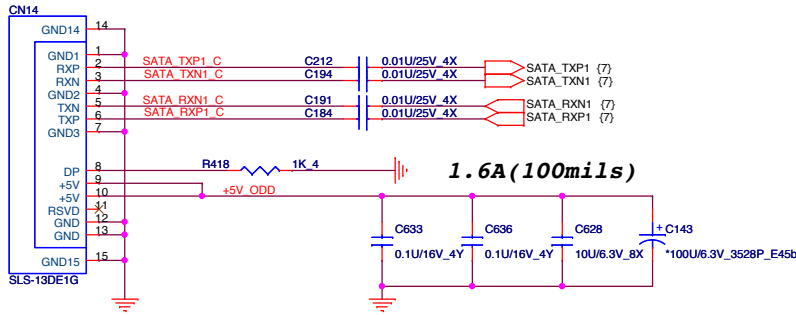
1.57 Low Power &gt;A:004 51 03

3.3V Low Power =>AL004951004

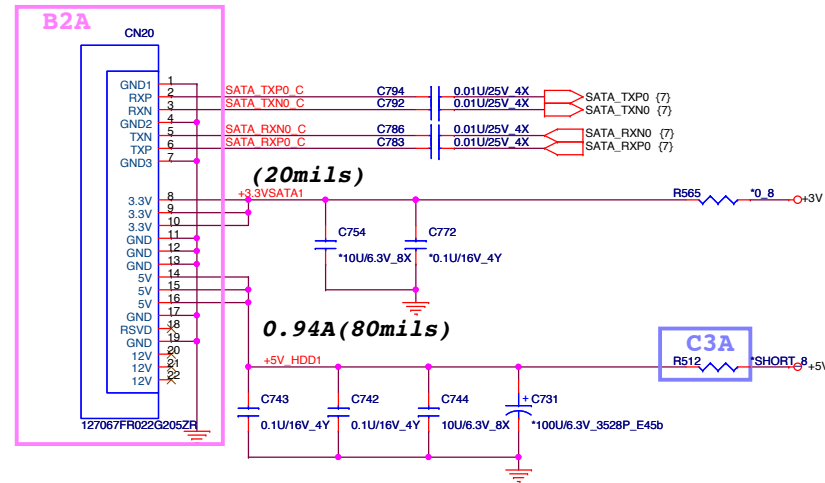


**ESATA CONN**

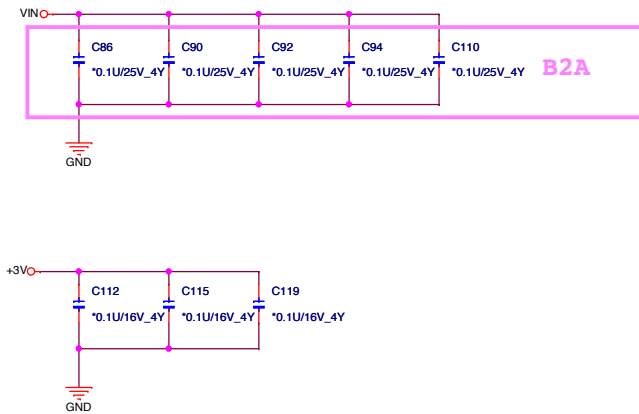


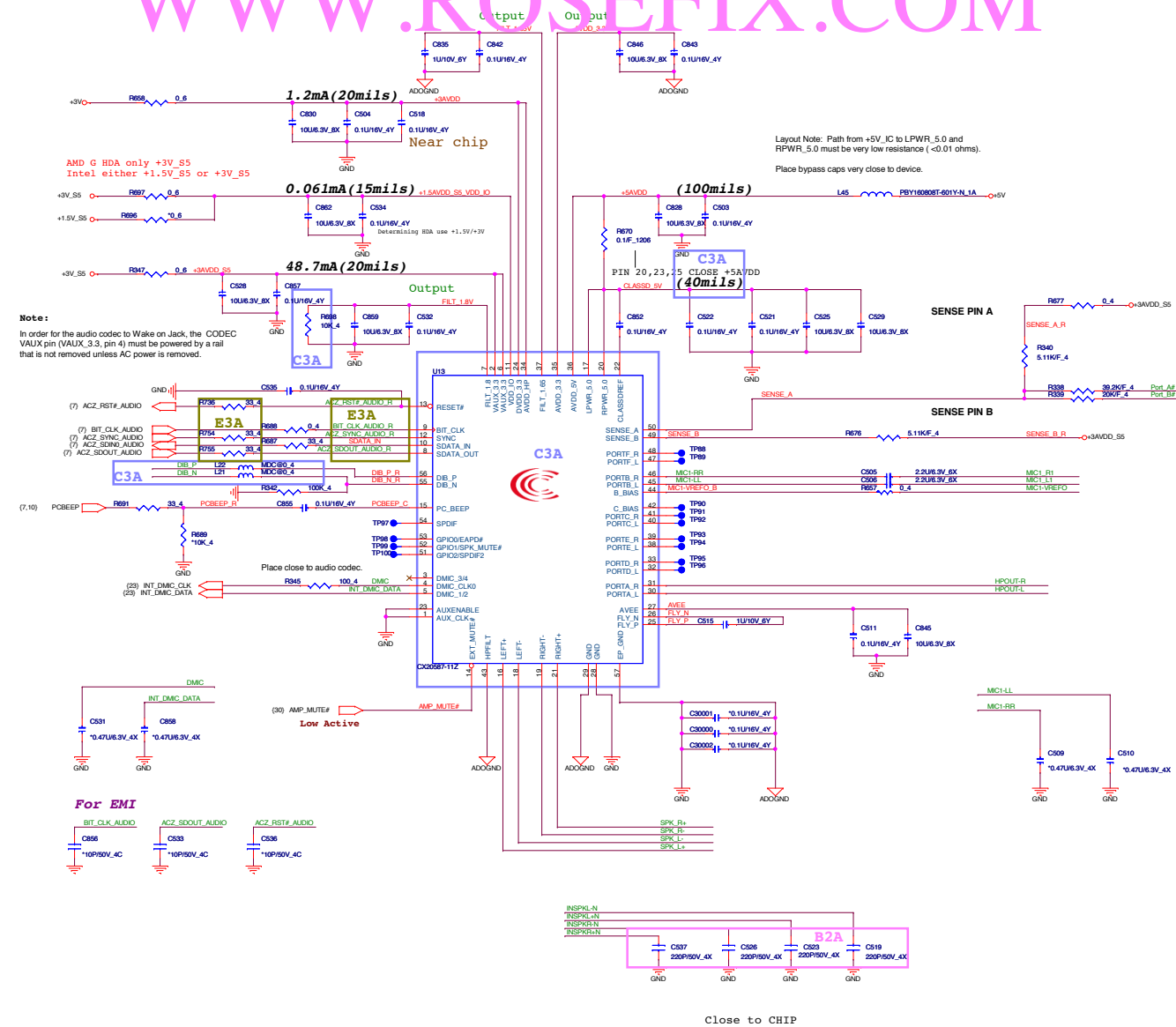


SATA HDD



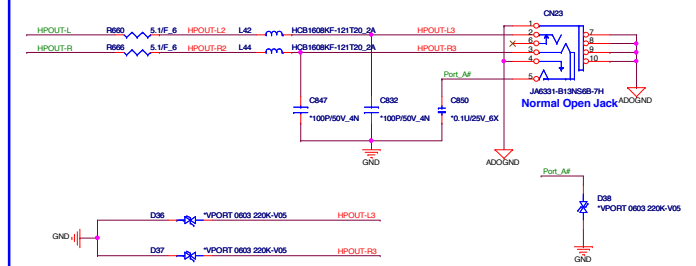
EMI



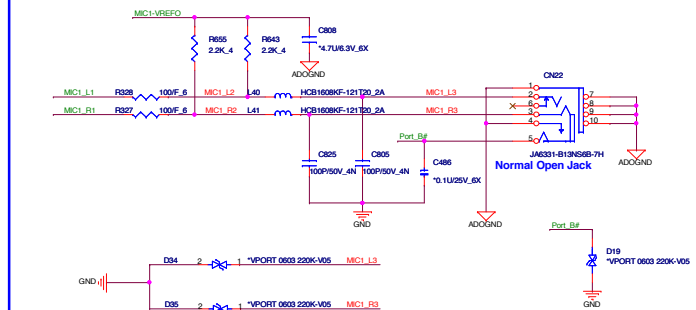


## AUDIO JACKS

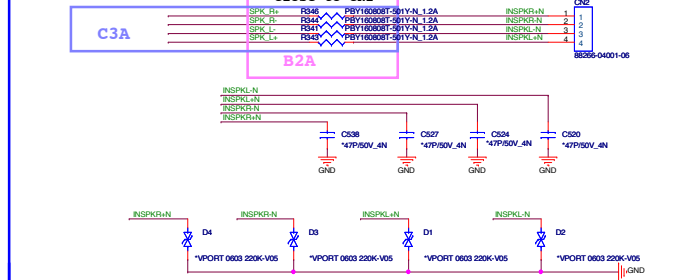
### Earphone



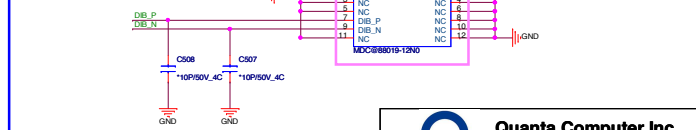
### External MIC

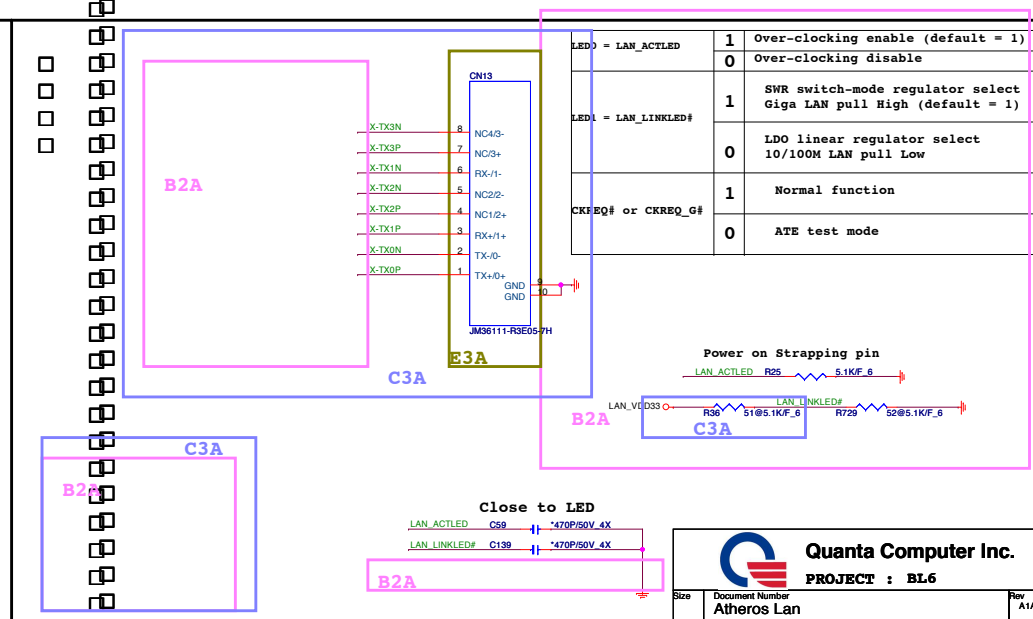
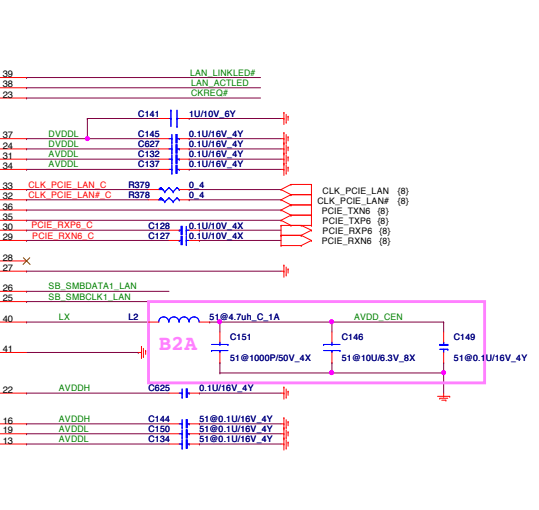


### Internal Speaker

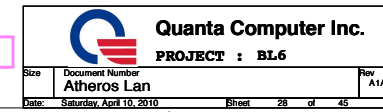


### MDC



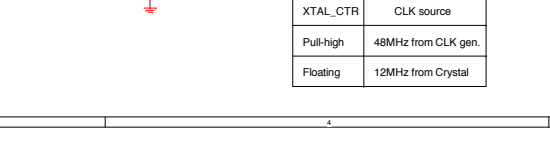
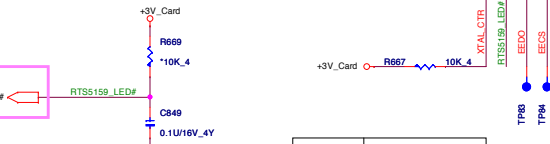
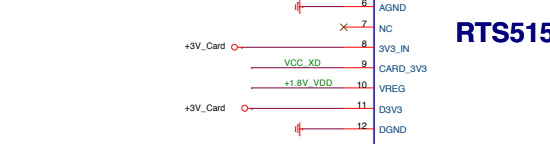
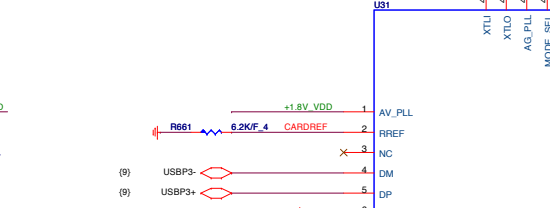
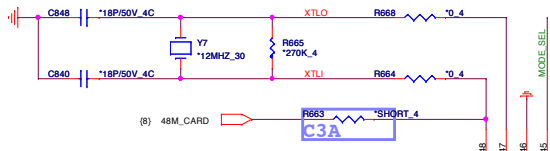
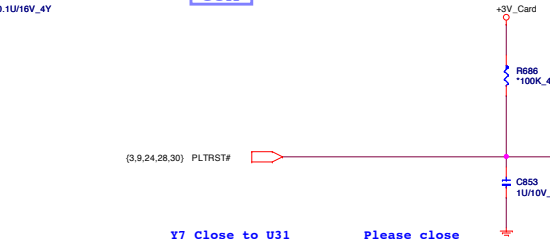
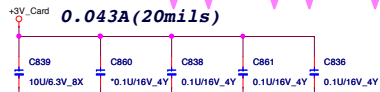
[illegible]

LAN\_ACTLED C59 \*470P/50V 4X  
LAN\_LINKLED# C139 \*470P/50V 4X



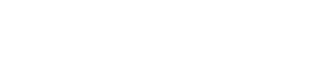
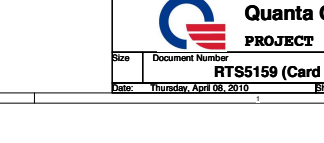
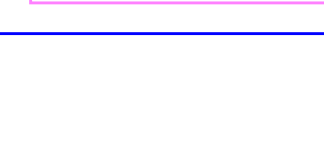
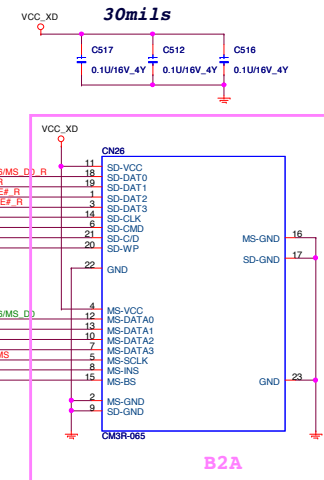
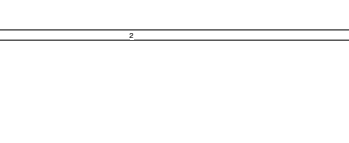
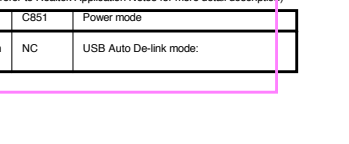
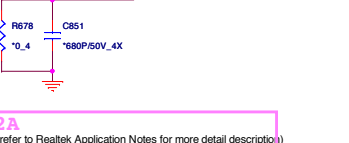
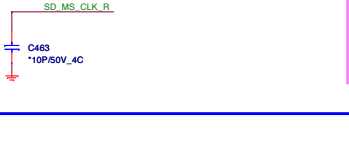
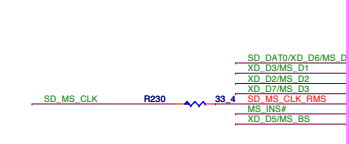
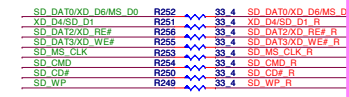


# 5 IN 1 CARD READER



WWW.ROSEFIX.COM

# 3 IN 1 CARD READER

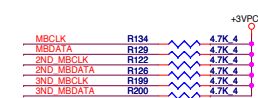
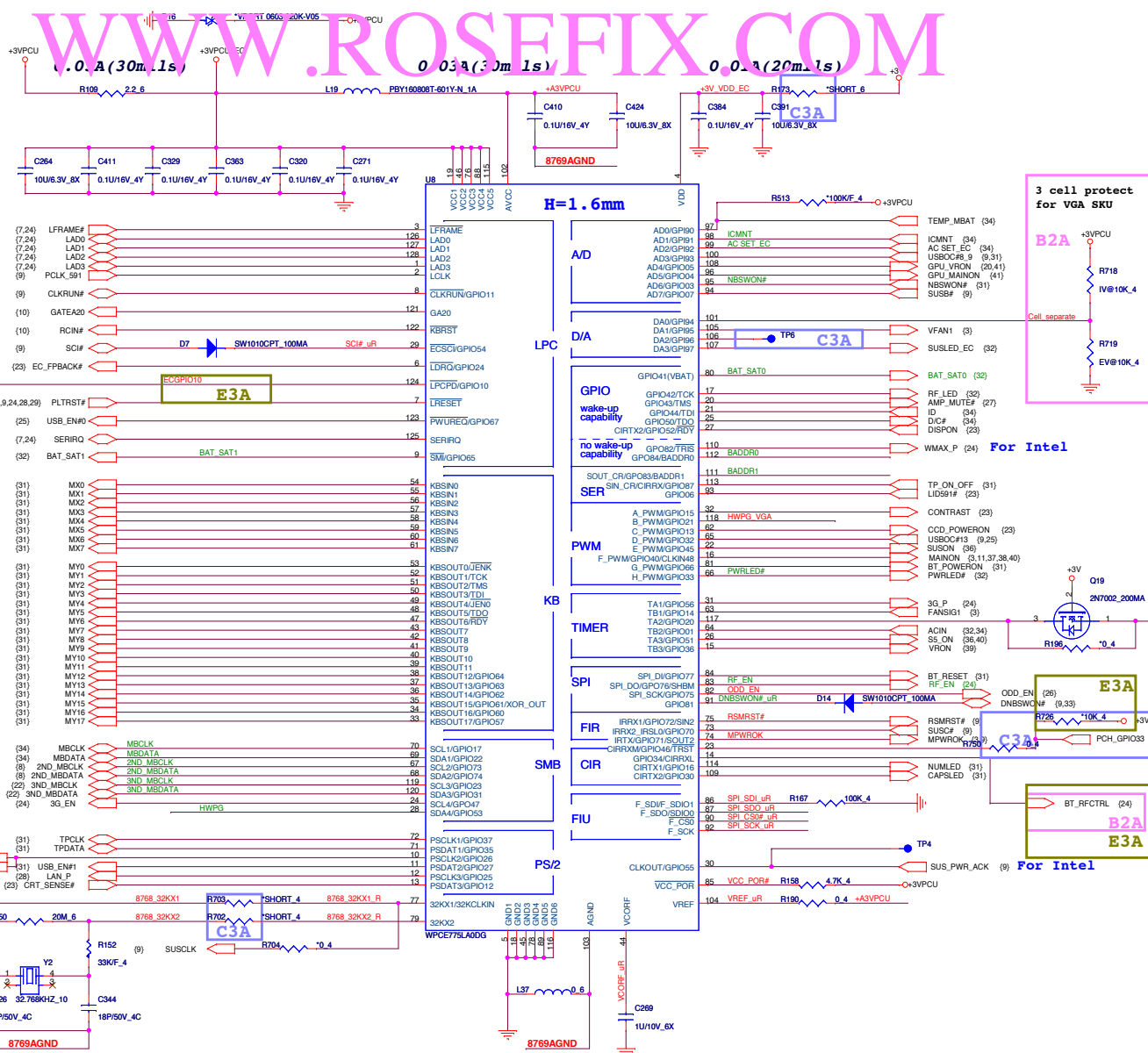


XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

MODE_SEL	R678	C851	Power mode
RTS5159	0-ohm	NC	USB Auto De-link mode:

**Quanta Computer Inc.**  
PROJECT : BL6

Size Document Number  
**RTS5159 (Card Reader)**  
Date: Thursday, April 06, 2010 Sheet 29 of 45



## I/O Base Address

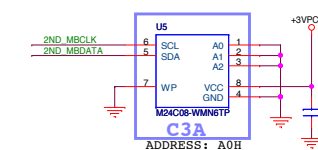
I/O Address		
BADDR1-0	Index	Data
0 0		XOR TREE TEST MODE
0 1		CORE DEFINED
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHIM: Enable shared memory with host BIOS



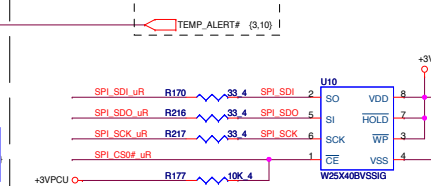
Disabled (1) if using FWing device on LPC.  
Enabled (0) if using SPI flash for both system BIOS and EC firmware

## ID



## SPI FLASH

For Intel

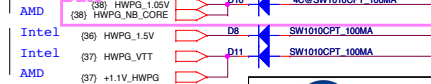
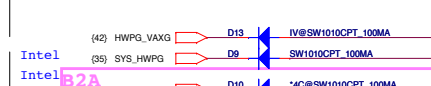
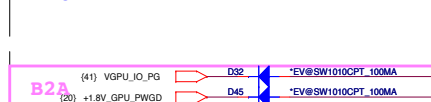


Intel	512KB	W25X40BVSSIG
AMD	2MB	W25Q16BVSSIG

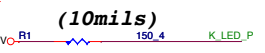
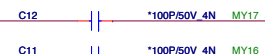
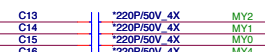
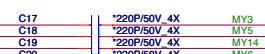
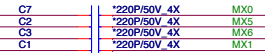
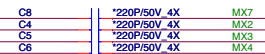
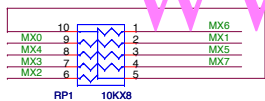
## INTERNAL KEYBOARD STRIP SET



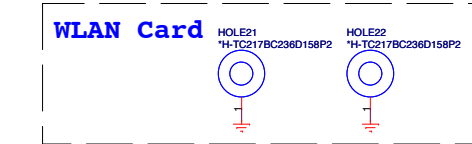
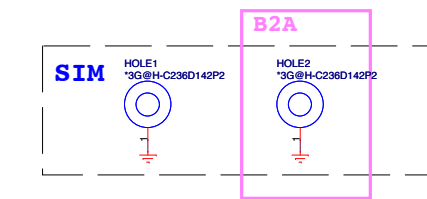
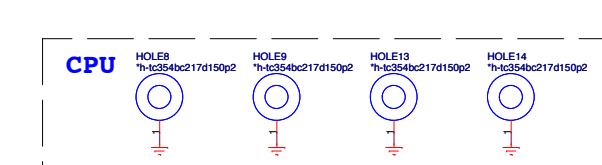
## HWPG



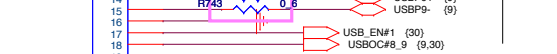
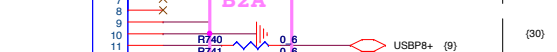
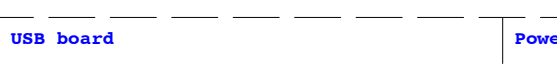
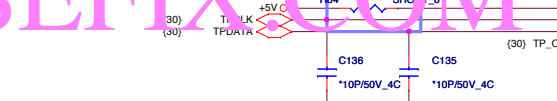
# INT Keyboard



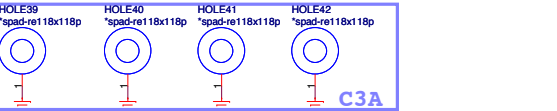
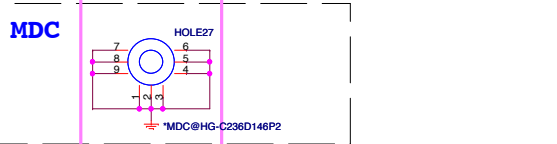
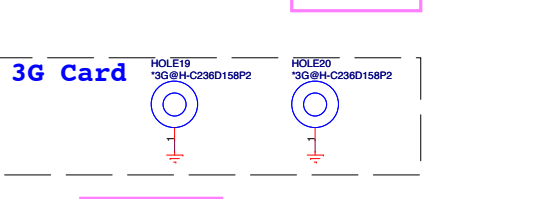
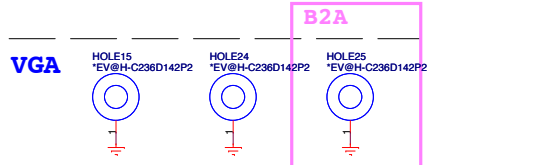
# NUT



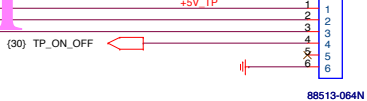
# TI board



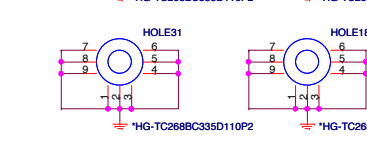
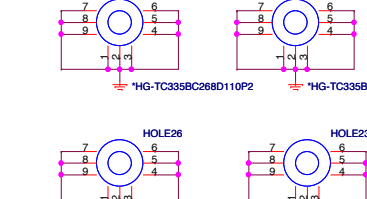
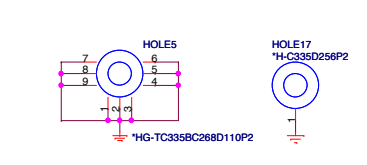
# USB board



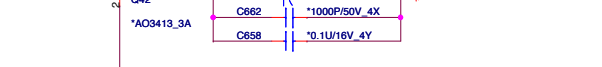
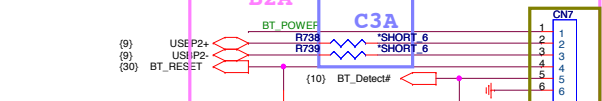
# Power board



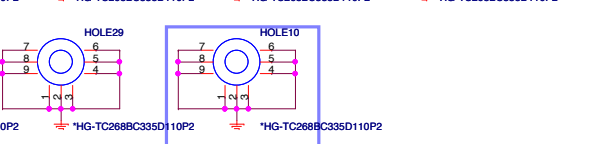
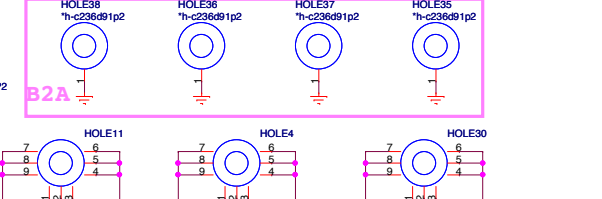
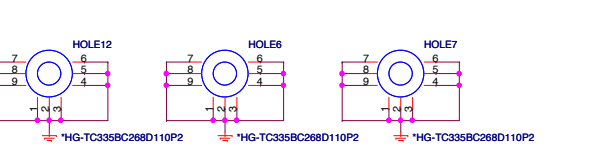
# Bluetooth



# Bluetooth

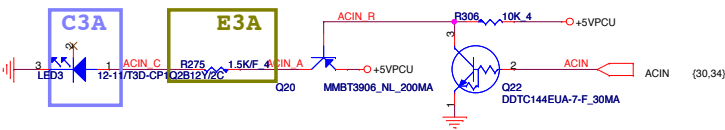


# HOLE

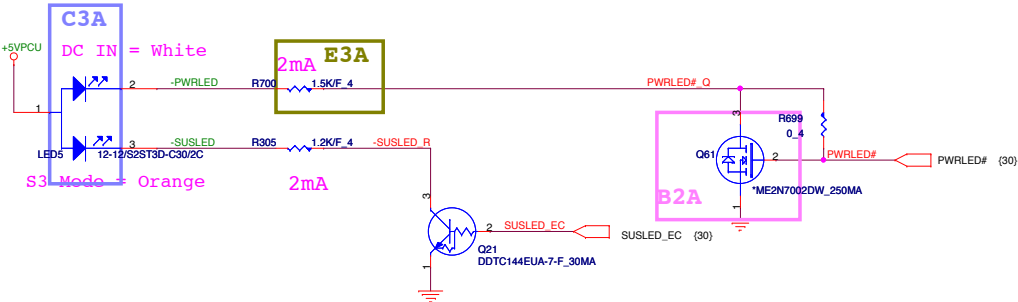


## LED

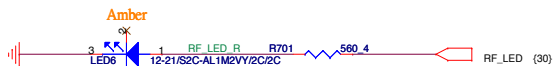
## AC-IN



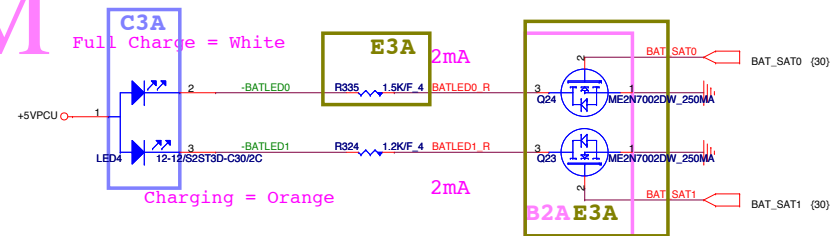
## POWER



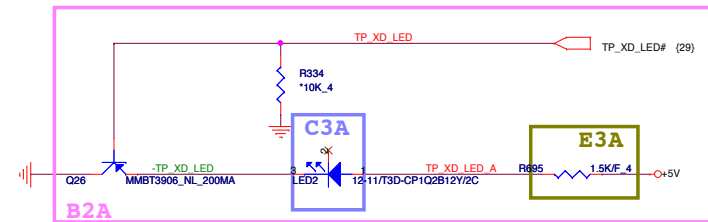
## RF LED



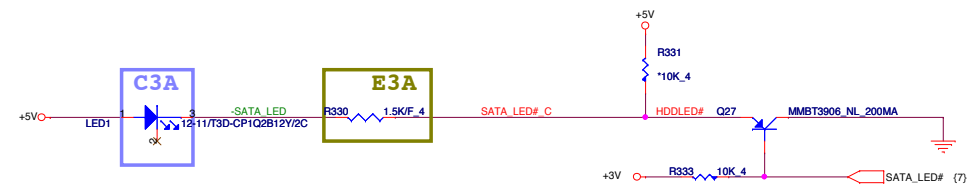
## BATTERY



## CARDREADER

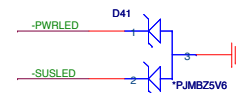


## HDD/ODD

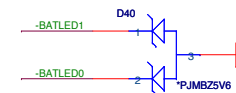


## ESD Protect

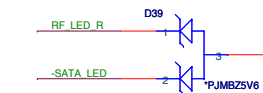
## FOR POWER LED



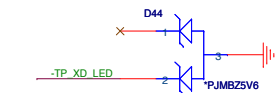
## FOR BATTERY LED

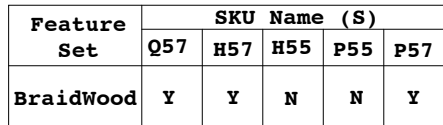


## FOR HDD/RF LED



## FOR CARDREADER LED

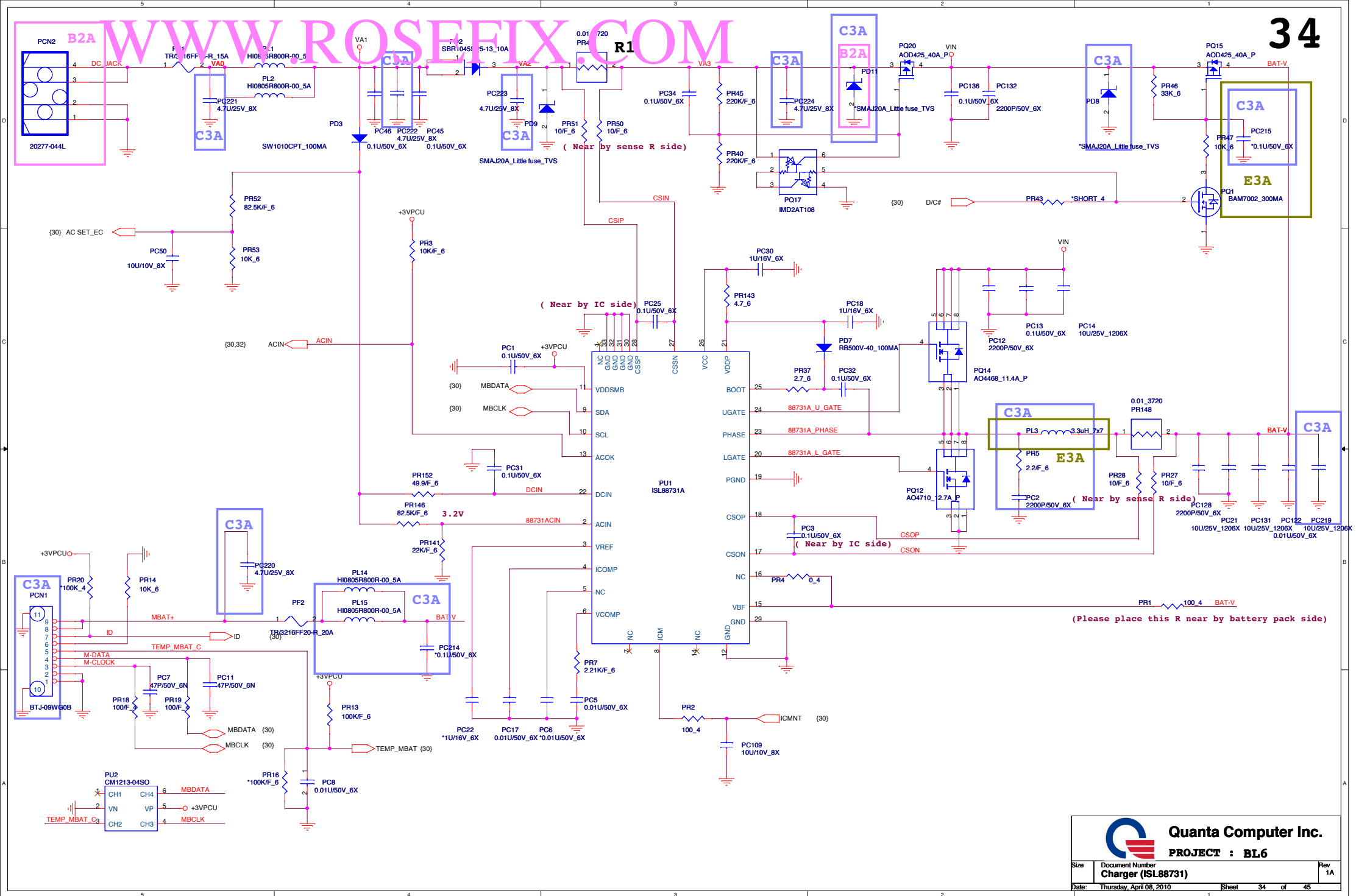




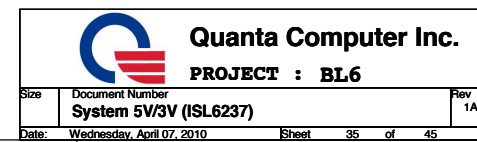
**Note: For ES1/ES2 version all stuff  
Production version all No stuff**

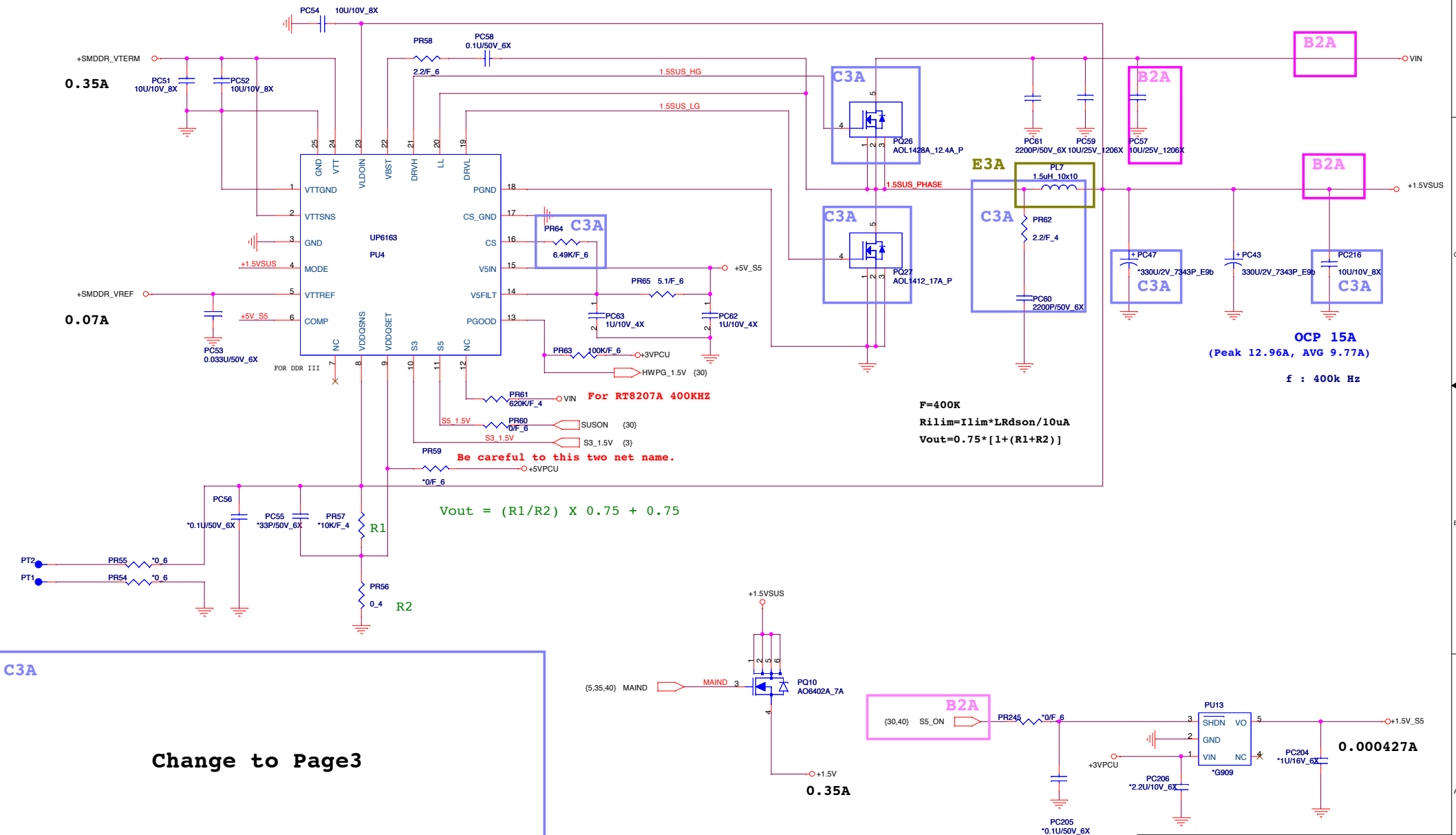


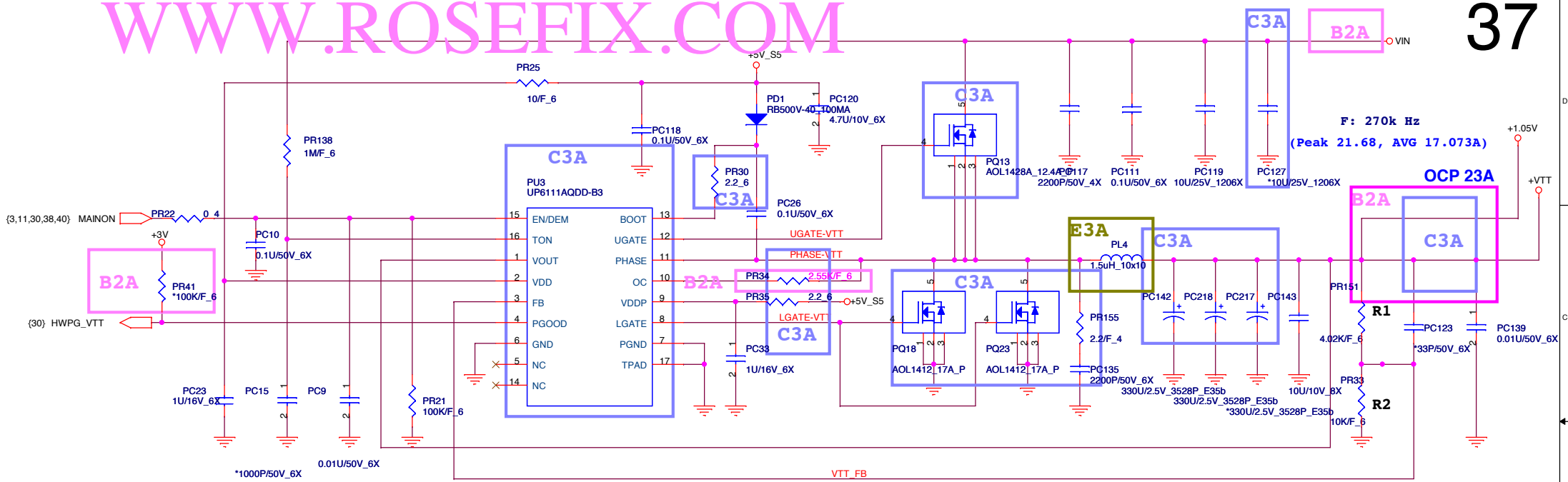




4.253A  
www.vinafix.vn







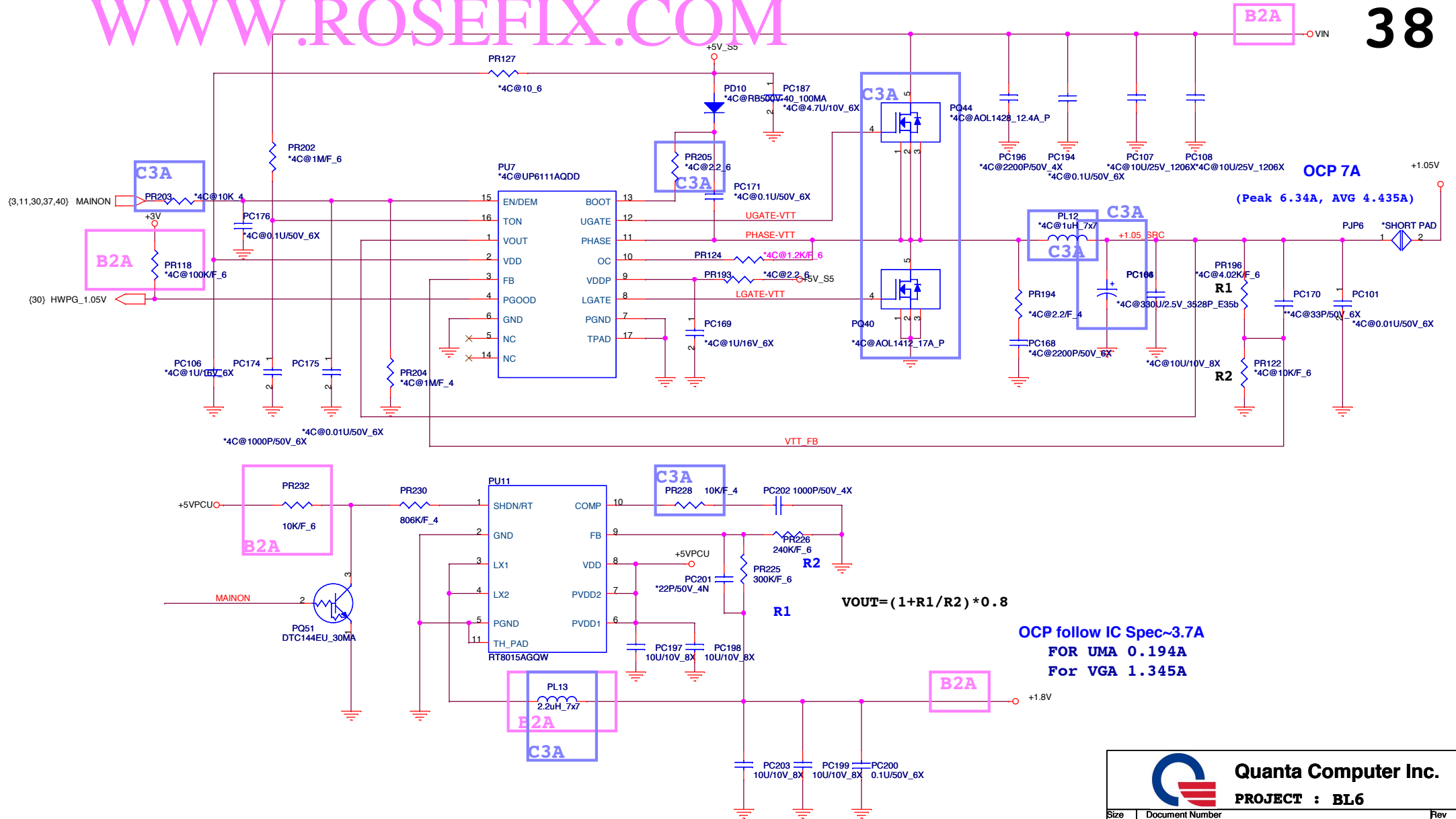
$$VOUT = (1 + R1/R2) * 0.75$$




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